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SPACE ADAPTATION
OF
ACTIVE MIRROR SEGMENT CONCEPTS

FINAL TECHNICAL STATUS REPORT

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711 SOUTH TEJON STREET, SUITE 202B

COLORADO SPRINGS, CO 80903

ON:

CONTRACT NAS8-40808

FOR:

CONTRACT ADMINISTRATION OFFICE

NATIONAL AERONAUTICS AND

SPACE ADMINISTRATION (NASA)

GEORGE C. MARSHALL SPACE FLIGHT CENTER

MARSHALL SPACE FLIGHT CENTER, AL 35812

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EXECUTIVE SUMMARY

This report summarizes the results of a three year effort by Blue Line Engineering Co. to advance the state of segmented mirror systems in several separate but related areas. The initial set of tasks were designed to address the issues of system level architecture, digital processing system, cluster level support structures, and advanced mirror fabrication concepts. Later in the project new tasks were added to provide support to the existing segmented mirror testbed at MSFC in the form of upgrades to the 36 subaperture wavefront sensor. Still later, tasks were added to build and install a new system processor based on the results of the new system architecture.

The project was successful in achieving a number of important results. These include the following most notable accomplishments:

- 1) The creation of a new modular digital processing system that is extremely capable and may be applied to a wide range of segmented mirror systems as well as many classes of Multiple Input Multiple Output (MIMO) control systems such as active structures or industrial automation.
- 2) A new graphical user interface was created for operation of segmented mirror systems.
- 3) The development of a high bit rate serial data loop that permits bi-directional flow of data to and from as many as 39 segments daisy-chained to form a single cluster of segments.
- 4) Upgrade of the 36 subaperture Hartmann type WFS of the PAMELA testbed at MSFC resulting in a 40 to 50X improvement in SNR which in turn enabled NASA personnel to achieve many significant strides in improved closed-loop system operation in 1998.
- 5) A new system level processor was built and delivered to MSFC for use with the PAMELA testbed. This new system featured a new graphical user interface to replace the obsolete and non-supported menu system originally delivered with the PAMELA system. The hardware featured Blue Line's new stackable processing system which included fiber optic data links, a WFS digital interface, and a very compact and reliable electronics package.

The project also resulted in substantial advances in the evolution of concepts for integrated structures to be used to support clusters of segments while also serving as the means to distribute power, timing, and data communications resources. A prototype cluster base was built and delivered that would support a small array of 7 cm mirror segments. Another conceptual design effort led to substantial progress in the area of laminated silicon mirror segments. While finished mirrors were never successfully produced in this exploratory effort, the basic feasibility of the concept was established through a significant amount of experimental development in microelectronics processing laboratories at the University of Colorado in Colorado Springs. Ultimately lightweighted aluminum mirrors with replicated front surfaces were produced and delivered as part of a separate contract to develop integrated segmented mirror assemblies.

Overall the project was very successful in advancing segmented mirror system architectures on several fronts. In fact, the results of this work have already served as the basic foundation for the system architectures of several projects proposed by Blue Line for different missions and customers. These include the NMSD and AMSD procurements for NASA's Next Generation Space Telescope, the HET figure maintenance system, and the 1 meter FAST telescope project.

BACKGROUND

The initial motivation for the work carried out under this contract grew out of various NASA initiatives to propagate high energy lasers through Earth's atmosphere to distant space-based targets. These initiatives were funded through the Advanced Concepts Directorate at NASA Headquarters, Code X, which has since been dissolved through organizational restructuring. While the appeal of directed energy concepts has gone in and out of favor within NASA several times over the past two decades, the goals of the missions that led to this research were bold and far reaching. The first, known as SELENE, sought to use Earth based free electron lasers to beam a near continuous source of multi-megawatt power to the lunar surface. The goal being to help boot-strap the colonization and industrialization of the Moon.

The second initiative was referred to as ULTIMA. The goal of this initiative was to beam energy to satellites for a broad range of missions. The key to both SELENE and ULTIMA, as well as many other efforts to propagate high energy lasers up through the atmosphere, is the existence of a large aperture beam director capable of adaptive control of the outgoing wavefront to pre-compensate for atmospheric effects. This requires beam directors on the order of 10 meters in diameter which possess the ability to modulate the wavefront at spatial scales of a few centimeters and at temporal frequencies of a few hundred Hertz.

For a 10 meter beam director this leads to an adaptive optics system composed of many thousands to several tens of thousands of subapertures, depending on the operating wavelength of the laser and the severity of the atmospheric turbulence at the time and location of the propagation. The sheer number of correcting elements far outstrips conventional approaches to adaptive optics, most of which are based on the use of relatively small deformable mirrors with (typically) no more than a few hundred subapertures.

As early as 1993 NASA personnel at the George C. Marshall Space Flight Center came to recognize the enormous potential of segmented active and/or adaptive optics technology. At about this time the PAMELA Testbed was transferred from an inter-agency DoD program to NASA. Through considerable effort the NASA personnel at MSFC managed to take the PAMELA Testbed from a barely operational state to a leading edge demonstration of segmented optics technology. Yet as of 1995, segmented optics remained a relatively undeveloped technology. Few other organizations (if any) were looking into segmented mirror technology at this scale.

MSFC personnel recognized that further system level development was needed in order to provide a framework for contributions by others. Therefore one of the main objectives of this contract was to address the system level architectural issues and to design a core processing system that could address the controlled operation of thousands of active mirror segments. A second objective of the initial contract was to address the issues of how one physically supports arrays of mirror segments and how one distributes the power, timing, and data signals needed for their operation. This led to the notion of an integrated structure referred to as a Cluster Support Base.

In 1995 a project was set up that involved SY Technology Inc., Georgia Tech Research Institute, China Lake, Blue Line Engineering Co., and others. The focus of the SY Technology effort was to develop an inductive edge sensor technology based on LIGA fabricated coils and single IC signal conditioning electronics. GTRI was to support SY Technology in attaching the

edge sensors to the edges of hexagonal mirror faceplates measuring 7 cm flat-to-flat. GTRI was also tasked with addressing the issues of flexible electronic interconnects between the mirror faceplate and the segment electronics mounted behind the faceplate. The US Naval Air Warfare Center at China Lake was tasked with designing and fabricating a small batch of mirror faceplates based on inputs from the rest of the project group. One of Blue Line's tasks was to provide China Lake with basic design specifications. As it turned out the SOW for this research states that Blue Line is responsible for designing and fabricating mirror faceplates, as will be discussed in this report. Blue Line was responsible for the system issues mentioned in the preceding paragraph. Also, the results of a parallel effort funded through a Phase II SBIR award to Blue Line were intended to dovetail with the other efforts to result in a portable technology demonstrator known as the Seven Segment Demonstrator.

In recent years the interest in directed energy concepts has all but disappeared within NASA. At the same time, various organizations within the Department of Defense have renewed research in this area for a variety of ground-based, airborne, and space-based missions. There is also a renewed push towards large aperture space-based imaging systems within the DoD and other Government agencies. Thus, the potential benefits of segmented mirror technology to many future NASA missions outside the area of directed energy have been recognized. Segmented optics is also becoming widely accepted within the astronomical community as the most viable means to construct telescopes with primary mirrors of 10 meters and larger. While Blue Line sees little commercial interest in 7 cm scale active segmented mirror systems at this time, the results of this and other research at Blue Line are directly applicable to a wide range of missions of national importance, including current efforts to develop a successor to the Hubble Space Telescope.

Statement Of Work

The SOW was modified three times in the course of this contract to incorporate new tasks as the project progressed. These tasks were designed to allow independent research being carried out at MSFC by NASA personnel to make use of the latest developments in this project. A full statement of the final SOW follows:

Task 1 — Next Generation Segment Controller

Contractor shall design, develop, prototype, test, and demonstrate the next generation of digital processing hardware and software for PAMELA class segmented optics. The plan is to review, revise as necessary, and implement the basic architectures first proposed at the 1994 SPIE OE/LASE Conference. Contractor shall provide technical expertise in conjunction with MSFC efforts to upgrade the existing PAMELA wavefront sensor and incorporate these efforts into the development of the next generation controller.

Contractor shall design, build, test, and deliver three prototype wavefront sensor assemblies in support of MSFC efforts to upgrade the existing wavefront sensor on the PAMELA testbed and build, test, and deliver a full complement of 36 wavefront sensor assemblies based on the results of NASA's evaluation of the three prototypes.

The contractor shall develop, install, and test a third generation segment controller for the PAMELA testbed. This additional controller shall include processing electronics and user

interface software upgraded from the next generation controller. The contractor shall rehost the segment control code from the PAMELA processor to the third generation processors and the contractor shall replace the wavefront sensor digital interface boards. The contractor shall perform on-site integration and testing of the third generation controller in the PAMELA testbed at MSFC.

Task 2 — Develop Concepts for Cluster Mounting Base

Refine concepts for supporting an array of mirror segments. The array would constitute a subset of the full aperture, i.e. a cluster of segments. The cluster design shall integrate structural support requirements, controls, and electronics processors (including the Task 1 Controller) and networks, electrical power management and distribution, and mechanical alignment and calibration methodologies. Various materials and methods of construction shall be identified and compared. A recommended design shall be produced.

Task 3 — Mirror Technology Development

Refine concepts for fabricating, coating, and finishing small hexagonal mirrors. Produce and analyze a mechanical design. Produce eight (8) finished mirror segments and test for optical quality. The eight segments are for an array of seven plus one spare. The mirrors should be appropriately scarred for attachment of flexures, edge sensors, and other typical adaptive mirror segment components.

Scope of This Report

This report will provide a summary review of the work that was conducted under NASA contract NAS8-40808.

Sources of Additional Information

Interested parties should contact Blue Line Engineering Co. for additional information:

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www.active-optics.com web site

The NASA technical point of contact for this research was Edward E. (Sandy) Montgomery at the Marshall Space Flight Center in Huntsville, AL. (phone 256-544-1767)

Several relevant papers appeared in the SPIE Proceedings on Laser Power Beaming, Vol. 2121, 27-28 January 1994.

PROJECT REVIEW

In the following pages we will discuss each task and subtask separately. This is being done in the hope that it will prevent the sort of confusion that could result from such a wide range of subject matter. In each case we will discuss what was done, what was accomplished, problems encountered, lessons learned, and conclusions or recommendations.

In some portions of the discussions which follow we will make reference to the Seven Segment Demonstrator or SSD. This is due to the fact that the results of some of the work being carried out under this contract were intended to feed into the SSD project along with the results of several other contractors as mentioned in the preceding section.

Task 1.1 — Next Generation Segment Controller: System Design & Development

System Architecture

Segmented active optics systems typically result in the need to process data from a large number of sensors at high throughput rates to control large numbers of actuators. Such systems are generically referred to as Multiple-Input Multiple-Output (MIMO) control problems. Commercially available processing hardware is expensive, bulky, and does not address the difficult problem of getting large amounts of data into and out of the processor at high rates.

NASA currently operates a segmented telescope testbed at the Marshall Space Flight Center which utilizes an early prototype of a parallel processing system referred to as an Extendable Digital Processor (EDSP). While the basic architecture of that system is sound, a new generation of processing hardware and software was needed for several reasons. First, the existing hardware is unreliable due to many modifications repairs needed to make the prototype boards functional. Since that hardware was custom made for that testbed and is no longer supported by the original manufacturer, repair or replacement of defective or intermittent hardware is not an option. In addition, the existing EDSP system is based on a 9U height VME backplane, which results in a very large hardware format that is unsuitable for space-based experiments. (See Figure 1)

For the next generations of segmented optics systems, an entirely new system processor has been developed. A block diagram is presented in Figure 2: Baseline System Architecture. At the head of the system sits the executive level processor, in this case referred to as the System Operations Computer which may be a laptop computer. This executive level processor provides a graphical user interface between the human operator and the distributed control processing system. Alternatively the system could receive commands from a host processor such as a flight control computer. A variety of standard interfaces may be used to communicate these commands to the system. The current hardware employs a serial data link.

Just below the executive level processor, in terms of the system hierarchy, sits the module labeled System Control Processor (SCP). The function of the SCP is to coordinate the operation of a bank of parallel digital signal processor based modules referred to as Cluster Control Processors (CCP) and other auxiliary modules connected to a parallel data bus backbone. The SCP also handles a wide variety of mission specific tasks as well as telemetry extraction, general health and status monitoring, downloading and initialization, and master timing.

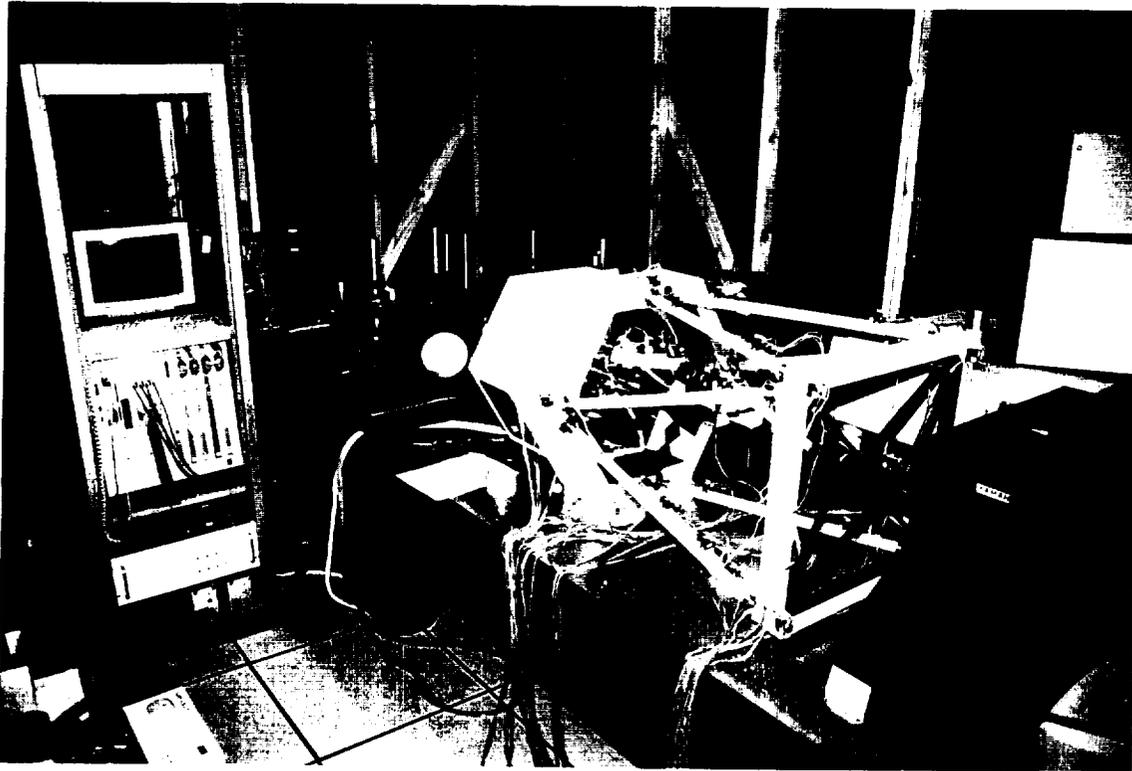


Figure 1: PAMELA Testbed at MSFC. The system controller is the large electronics module in the middle of the equipment rack to the left.

As mentioned above, the SCP communicates with a bank of processing modules referred to as CCPs. Each CCP is essentially a high speed dedicated processing unit which handles some reasonable grouping of sensors/actuators/subsystems which we refer to as a cluster. A block diagram of a CCP is presented in Figure 3: Cluster Level Processor Block Diagram.

The exact size of a cluster depends on a number of factors and the decisions made by the system designers. The upper limit on the size of a cluster is determined by at least three factors: the bandwidth of the high speed serial communications paths, the frame rate (currently set at 5,000 Hz), and the number of bits per node per frame (currently at 48 bits/node). Another factor which limits the practical size of a cluster is the amount of processing to be performed on each data value in each frame. In a totally distributed control system the CCP does little but extract telemetry data and issue commands. In such cases one could form clusters of as many as 1250 nodes (e.g. active mirror segments). In practice the size of a cluster is likely to be considerably lower than that number, perhaps 400 or less. Most likely the cluster size will be based on mechanical considerations. In fact, the original notion of the cluster grew out of the recognition that it was impractical to assemble very large segmented mirror arrays unless one breaks them down into physically manageable clusters.

Referring to the Cluster Level Processor Block Diagram, the DSP selected for the CCP module is the Motorola 56301. This 24 bit processor is capable of 80 million arithmetic operations per second. This processor was selected after a thorough trade study in which both 16 bit fixed point

and 32 bit floating point processors were considered. Ten different control algorithms (for the segmented adaptive optics application) were evaluated in terms of memory requirements, processing time, power consumption, and complexity. The conclusion was that a 24 bit fixed point processor was ideally suited to applications where the precision of the sensors and actuators was 16 bits or less.

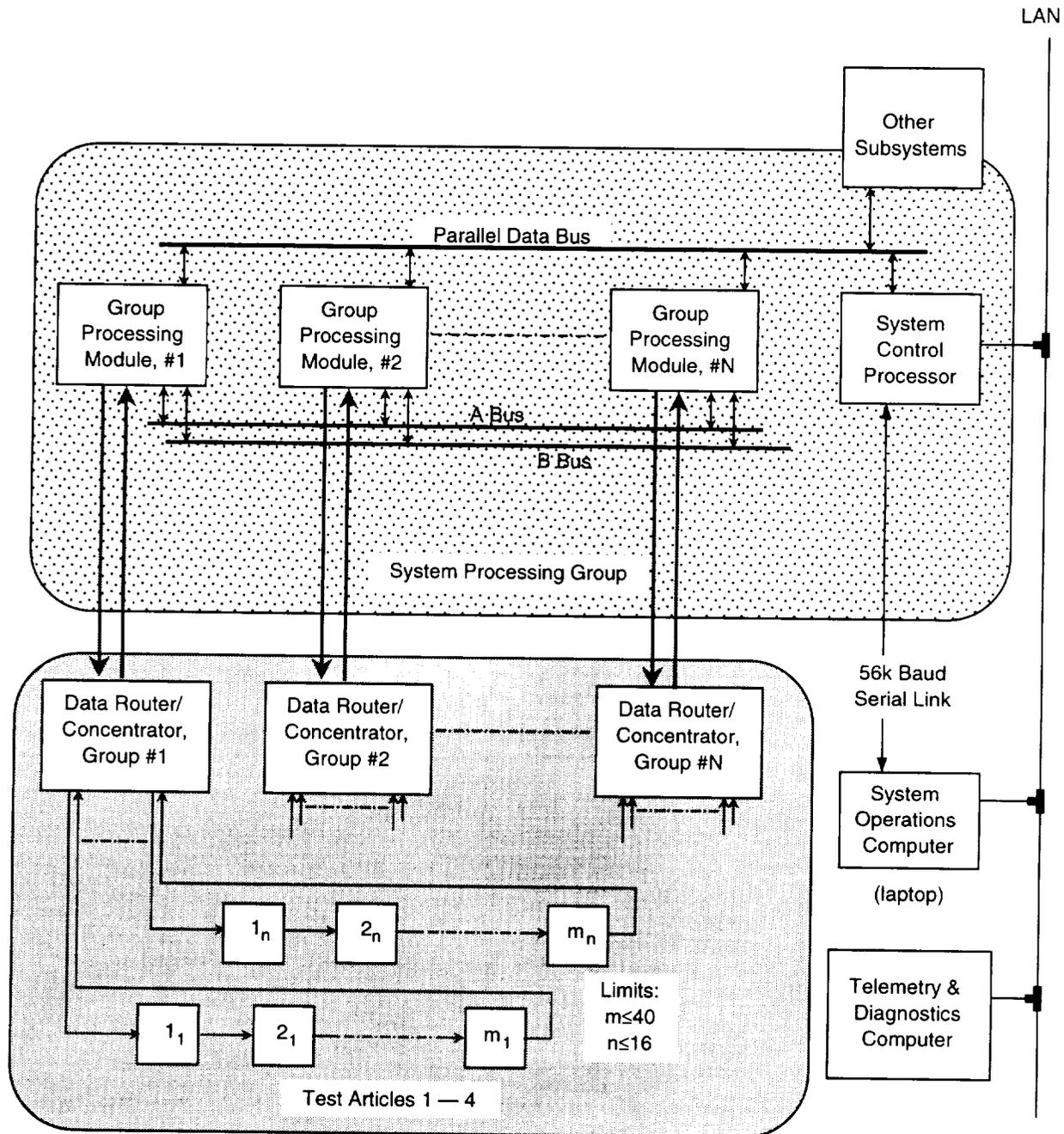


Figure 2: System block diagram

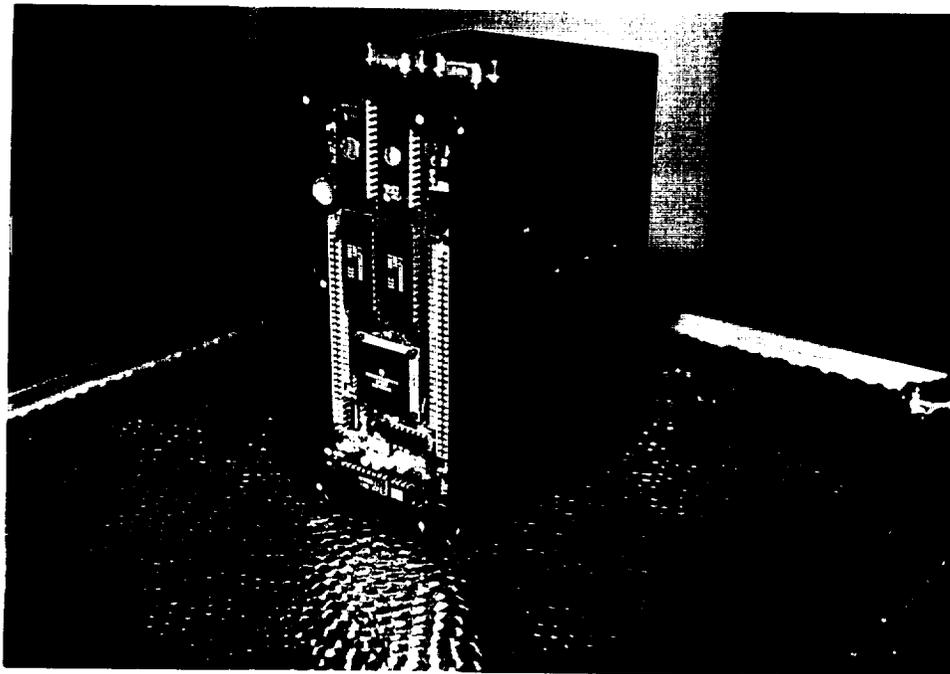
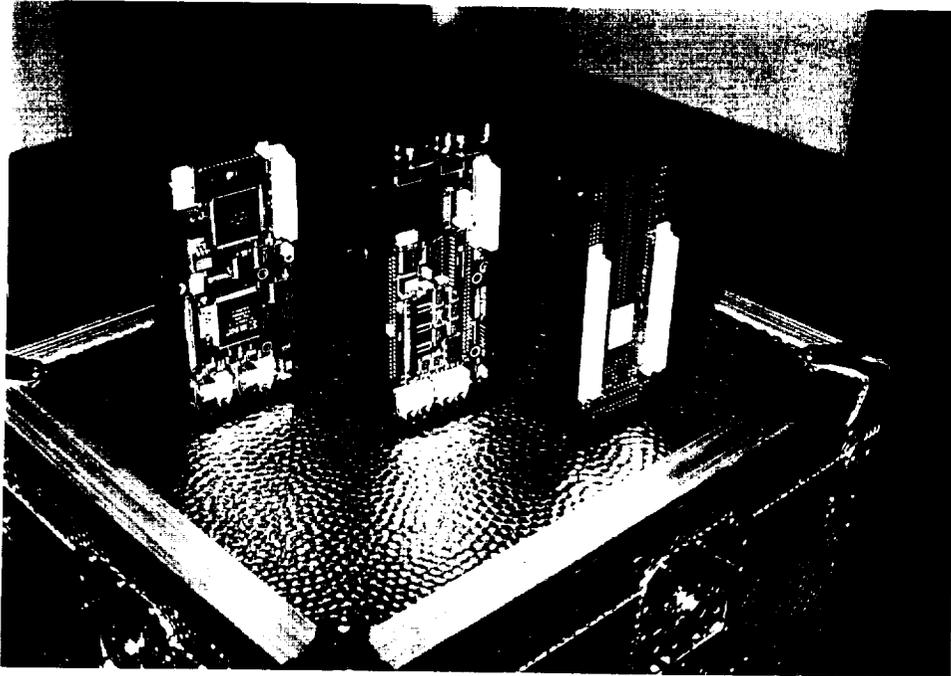


Figure 4: System Processing Modules. Upper photo shows CCP (left) and MTM front (center) and rear views (right). Lower photo shows assembled stack with one SCP followed by MTM and three CCPs.

Hardware and Software Description

The first implementation of this new generation of processing system was built for the SSD project (see photos, Figure 5). The SSD can be broken into three major components. The first is a laptop computer. The second is a collection of 3 computer boards that are collectively referred to as the "processing module". The third consists of the mirror segments and their associated

hardware and electronics. This section will focus on the more significant features of the new processing system. First, the electronics will be discussed in a hierarchical manner, starting with the operator interface, and working our way further and further into the system. After the discussion of the electronics is complete, a detailed description of the software for each component will be given.

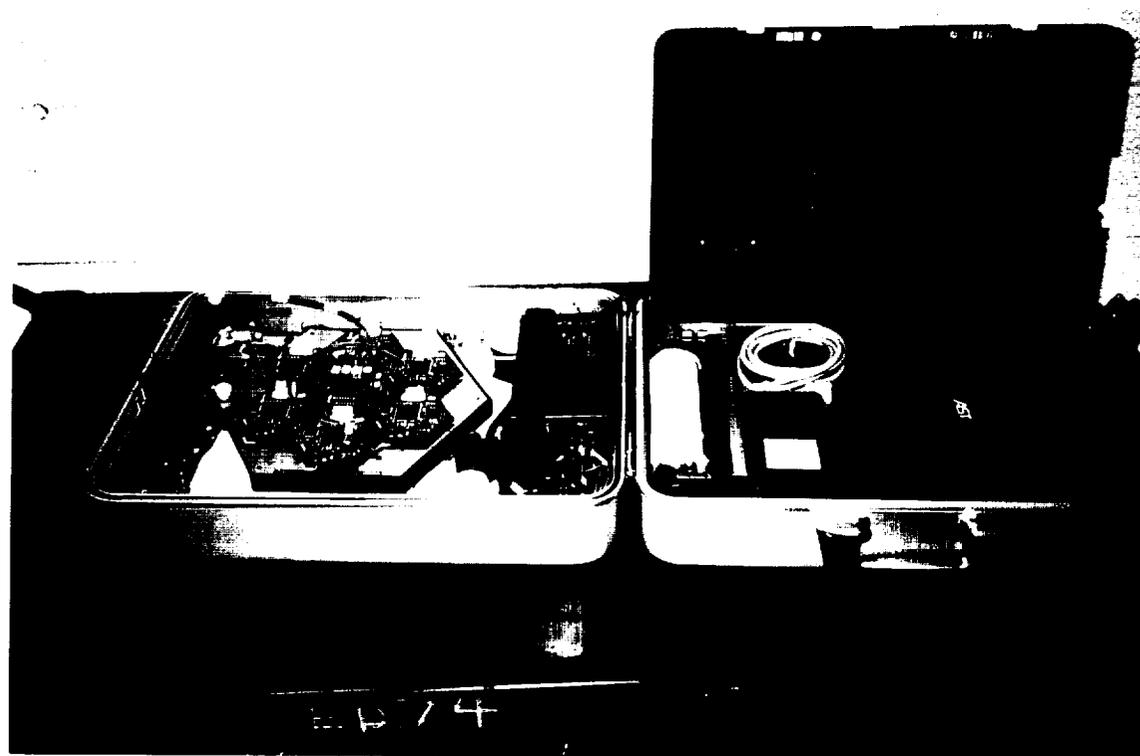


Figure 5: Seven Segment Demonstrator deployed for demonstration (upper). SSD in stowed position for transport (lower photo). Note the System Processor and Cluster Base in left compartment, laptop and power supply in right.

Laptop Computer

The element of the SSD that the operator will be most familiar with consists of an IBM-compatible personal computer. Specifically, an AST Advantage! Explorer laptop computer, running an Intel 80486 DX4/100 processor. The key feature of this laptop is the RS-232 serial data port. All communication with the SSD is via this interface. Based on this, nearly any computer, Macintosh or clone, could be used. An IBM-compatible computer was selected based on the fact that the preferred software development suite, Borland's Delphi, is only available for PC clones.

The software written for the laptop computer, Delphi, is a visual/object oriented language based on the Pascal programming language. Delphi allows the programmer to construct Windows-based applications that use all the point and click features present in a modern user interface. Upon starting the Seven Segment Demonstrator application, the operator will be presented with a menu that will allow complete control the system. This includes control the high speed serial data link, mode control, and manual control of each mirror segment. Each time the operator selects a button or menu item on the screen, an "event" is generated that is parsed by the underlying software. When the appropriate action to be taken is determined, a message is sent to the SCP via the RS-232 communications link where further action is taken. The laptop software is also responsible for collecting telemetry and status information on the SSD. This, and any other periodic processing is initiated by timers that can be setup to trigger processing as often as every millisecond. Modification of this software requires the Delphi programming suites, plus a detailed understanding of the use of this language.

Power Supplies

Electrical power for the SSD is provided by an off-the-shelf power supply from Advanced Power Solutions. This unit provides up to 5 Amps of +5vdc, and 1 Amp of -5vdc. This is sufficient for all elements of the SSD except the laptop computer, which has its own conventional power converter. The laptop computer also has batteries built in that should allow it to function for up to 3 hours without the use of it's AC converter. It is suggested that, whenever possible, a filtered 115vac power supply be used with the SSD to protect it's many components.

Processing Module: SCP

The System Control Processor (SCP) is a small off-the-shelf single board computer built around Motorola's 68332 microprocessor. This board acts as a high level coordinator for all SSD operations, and is responsible for processing commands from the operator via the RS-232 interface, and collecting telemetry. One SCP is required for each segmented mirror system.

The SCP requires ground and +5vdc power, on connector **J1**. This is the entry point for all digital power for the entire processing module block (consisting of the SCP, MTM, and CCP).

As mentioned, the SCP communicates with the PC via an RS-232 serial port. The data rate of this link is limited by the workload the SCP must perform. Currently, the maximum functional data rate is 9600 baud. At this setting, a bottleneck exists between the PC and the rest of the system, which is capable of collecting many megabits of telemetry data per second. For this

reason, the operator may only select a limited number of telemetry data points. The SCP also has a port that will allow the use of a "hand controller". This hand controller (not supplied with the SSD) consists of a numeric keypad and LCD display. In a simplified version, this hand controller could serve as an extremely simple operator interface to an adaptive optics system.

The SCP supports software development using Motorola's Background Mode Connector interface. From this port, a personal computer can be connected to facilitate software downloads and debugging. This connector is used only during software development, and is not used during routine operations of the SSD.

The software running on the SCP consists of telemetry and commanding utilities written in the "C" programming language. With only one cluster in the SSD, the processing performed by the SCP is relatively simple. The SCP will accept incoming data and commands from the laptop computer via the RS-232 link. When a command is received, the SCP parses it, and determines what processing must be performed. This processing generally includes recording any mode changes made, and forwarding the command to the CCP board(s). Periodically, the CCP will report telemetry and status to the SCP, which is then forwarded to the laptop, again, via the RS-232 link. The bulk of the processing performed by the SCP includes buffering the telemetry coming from the CCP(s), and streaming it to the SCP as quickly as the RS-232 data rate allows. Included in the "C" development suite from Software Development Systems, Inc. is a set of RS-232 utilities, plus provisions for handling interrupts. The interface going between the SCP and the CCP(s) is configured so the CCP(s) appear as any off-chip device at addresses defined by the wiring of the MTM board.

Processing Module: MTM

The Master Timing Module (MTM) is a custom board providing two major functions. First, it provides all clock signals used by the SSD, including a 10 MHz "master clock", and a 5 kHz "frame sync". These signals are used to clock data through the system, and to indicate the start of a new "frame". The second function of the MTM is to provide an electrical interface between the SCP and the CCP(s). The MTM also provides mechanical mounting points for the system power supply, and the RS-232 connection that ultimately goes to the SCP.

The clock signals generated by the MTM are derived from a 20 MHz oscillator, and are made available to the rest of the processor module through the stacking connector that connects to the CCP board(s). Fiber optic links are also provided to allow these timing signals to be sent to the segmented mirror array and an optional Wave Front Sensor (WFS). Provisions have also been made on the board to allow the use of BNC type connectors to access the master clock and frame sync signals. The polarity of the master clock can be switched as can the polarity of the frame sync signal going to the CCP stack. In addition, the phase delay for the master clock signal can be altered by setting jumpers on the MTM board. Also, the duration of the frame sync signal and the rate of the frame sync signal, nominally 5 kHz, may be altered by setting.

The MTM has a row of 4 LEDs that are accessible from the SCP. All are general purpose in use except for LED #1, which is used to control the frame sync signal. When LED #1 is in the "off" state, the frame sync signal is disabled, effectively terminating the flow of data on the 10 MHz fiber optic lines. When LED #1 is in the "on" state, the frame sync signal is enabled, turning on the 10 MHz fiber optic data stream.

The MTM has one additional feature of note, an expansion port. This port will allow the SCP to use other electronics not included with the SSD. Examples might include additional RAM or ROM, analog to digital or digital to analog converters, or other digital boards. This port is accessible only from the SCP using the data, address, and control lines available on the MTM.

Processing Module: CCP

The CCP is a custom computer board that controls the operation of a cluster of mirror segments. This board uses the Motorola 56301 Digital Signal Processor (DSP) and a Xilinx Field Programmable Gate Array (FPGA) which handles the 10 MHz serial data stream. Each CCP can communicate with up to 39 mirror segments via the 10MHz serial communications link. Additionally, a dual serial bus is also available between CCP boards, facilitating inter-cluster communication. A third (unused in the SSD) interface allows the reception of wave front sensor (WFS) data consisting of tip/tilt gradient information for each mirror segment in a cluster. The interfaces to the WFS and to the mirror cluster use plastic fiber optic elements, allowing large distances and reliable communications between the CCP and these other units. The CCP executes software written in Motorola's assembly language development suite.

The CCP has an on-board 33.0 MHz oscillator that is internally doubled to 66.0 MHz in the DSP. The DSP is a 24 bit device with built in memory (4k program space and 4k data space) and numerous interfaces. These interfaces include a JTAG port that allows downloading and debugging of software from any of a number of commercial interface boards, an unused Serial Communications Interface (SCI) port, two Enhanced Synchronous Serial Interfaces (ESSI) ports, a Host Interface (HI32) port, as well as external data and address lines.

The two ESSI ports are used to construct dual 22 MHz serial busses between CCP boards (A/B serial busses). All data and control lines are brought out on the stacking connectors to allow multiple CCP boards to communicate with each other. These busses facilitate inter-cluster communications, and are not used in the SSD with it's single cluster.

The a parallel data port (HI32) is used to allow the SCP board to communicate with one or more CCP boards. It supports a command vector mode where the SCP can directly initiate interrupt processing in any of the 256 DSP interrupts. This means that each CCP module must determine an "id" for itself upon startup in order to properly configure the host interface port. This will facilitate communication between the SCP and the CCP(s). The CCP id is determined by reading the settings on the id switches

The CCP also has a bank of 8 LEDs that are used for general purpose display and status presentation. These LEDs can be written to with no restrictions. Like the MTM, the CCP has one additional feature of note, an expansion port. This port will allow the CCP to use other electronics not included with the SSD. Examples might include additional RAM or ROM, analog to digital or digital to analog converters, or other digital boards.

The software running on the CCP is permanently loaded into an EPROM. Programming the CCP board works much like the SCP. Software is written in "C" and/or assembly using Motorola's DSP Development Software suite, and can either be written into EPROM and loaded upon power-up, or can be loaded and debugged interactively. In order to run interactively, a JTAG interface board must be used, e.g. the Motorola EVM56303 board. Using this interface, which connects to the serial port of a PC, it is possible to download and execute the CCP

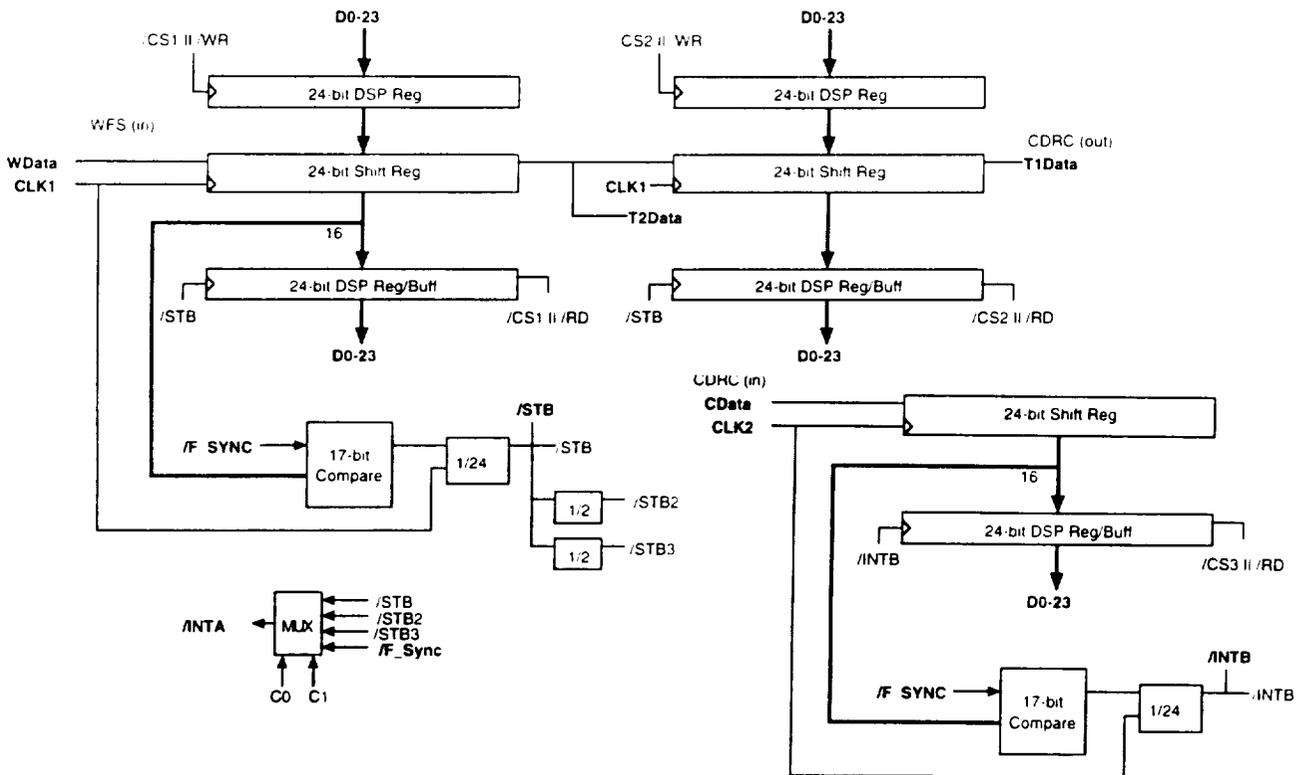
application software.

A second serial EPROM is used to program the FPGA upon power-up. The application running on the FPGA is tailored specifically for the SSD, and should not be altered.

Processing Module: CCP FPGA

The FPGA on the CCP is a programmable device that handles all high speed serial data travelling to/from the segmented mirror array. It is connected to two sets of fiber optics transceivers. 10 MHz data from the wave front sensor enters the FPGA through a pair of serial 24 bit shift registers. This data is then sent out to the segmented mirror array. After passing through the segment hardware, this data stream then returns, where it enters a 24 bit shift register, providing a communications loop between the CCP and it's segments. This serial data flow halts when the frame sync signal is asserted. At that time, the data in the shift registers, both at the CCP and segment levels, is available to be read by the DSP chip, and new outgoing data can be written in its place. When the frame sync signal is deasserted, the flow of the high speed data stream resumes. As data becomes available for the DSP, interrupts are generated to notify the DSP that the data registers are readable. All fiber optics devices used in the SSD are low cost parts using plastic (or silica) optical fiber. As supplied, 1 meter lengths of fiber are used, but longer lengths can be substituted.

The CCP(s) connect together using a set of stacking connectors. These connectors carry all signals required for the A/B serial busses between CCP, the host interface bus between the CCPs and the SCP, power and ground lines, clock signals, and several spare lines. The layout of this connector allows additional CCP modules to be added simply by snapping them into place (provided the appropriate jumpers and switch settings have been made).



The FPGA used on the CCP board is a custom application that handles the high speed serial data stream. Depending on how the FPGA is configured with control bits, words are extracted from and/or injected into the serial data stream every 24 or 48 bits. When this occurs, the DSP is interrupted, allowing the incoming/outgoing data to be serviced. This application has been created using a specialized toolset designed for FPGA application development.

The overall flow of data is shown entering from the fiber optic receiver into the 24 bit shift register B, continuing into the 24 bit shift register A, and then out to the fiber optic transmitter.

Processing Module: CDRC

The Cluster Data Router/Concentrator (CDRC) is a small custom circuit board that acts as data distribution hub between the CCP and a cluster of segments. It receives the high speed serial data stream coming from the CCP on fiber optics, and converts the signal to copper. The data is then sent out to the daisy chain of segment electronics, and ultimately returns back to the CDRC where it is converted back to fiber and sent back to the CCP. The CDRC also receives the 10 MHz clock, and the frame sync signal via fiberoptic links.

The CDRC monitors the serial data stream, watching for the "header" to return from the segment electronics. When this occurs, each segment has the data destined for it in its own shift register. The "shift" signal is now asserted, triggering each segment to read the serial data before it, and to place any outgoing data into the shift register. Once the shift signal is deasserted, the serial data begins clocking through the segments again.

The CDRC performs its processing using another Xilinx FPGA. As with on CCP, the FPGA programming is downloaded upon power-up from a serial EPROM. A second serial EPROM, is provided to allow a fixed test pattern to be injected into the high speed serial data stream. This feature is activated using a control bit in the serial data header word. A switch bank is used to set the number of segments in the cluster. By doing so, the CDRC can search for the fixed pattern in the header word over a small fixed window, providing a reliable filter to capture the head of the returning data stream during each frame.

Problems Encountered

One of the first hardware design tasks we completed was the design of the FPGA. This first design allowed serial communications at data rates of 162 MHz. But we soon discovered that the bandwidth was pushing the power, cost, and physical size of the processing boards and would have an equal effect on the rest of the system. This would be warranted if one were building very large mirror arrays, but it was clearly overkill for all of the near term applications we foresaw. So we elected to complete a second design based on a 10 MHz clock rate. This data rate would still allow one to control segmented arrays with up to 156 mirror segments with a four cluster System Processor.

Another issue we had to confront is the issue of system timing control. The system is designed as one big synchronous data system. There are two major considerations we had to address. The first is clock skew. The second is frame synchronization.

Clock skew comes about as a result of differences in the propagation delays of data streams vs. clock signals. By far the two most significant sources of propagation delay come about as a result of either the type and number of digital gates in the transmission path or the length and type of medium used to transmit the signals from one point to another. Our design rule is to maintain clock skew to $\pm 10\%$ of the clock period, which is ± 10 nanoseconds for the current system. For small systems, such as SSD or even the PAMELA testbed this requirement is easily met. For larger installations, such as what would be needed for the Hobby Eberly Telescope. The main consideration is to insure that the fiber optics cables relaying clock and data signals between the CCP and CDRC need to be kept equal in length to ± 3 meters or less.

It should be noted that for higher data rate systems, e.g. the 162 MHz design mentioned above, the clock must be recovered from the data stream itself. This is known as timing recovery. This need for timing recovery is part of the reason the higher bit rate design required more power and was more expensive. Also, in order to be able to send arbitrary streams of data, which may contain long sequences of ones or zeros, the timing recovery circuit needs to encode and decode the data to ensure that there are enough transitions in the data stream at all times to maintain synchronization of the local oscillator.

As noted, we have resolved all of these issues for now by switching to a slower clock speed (10 MHz) and shipping clock with data. If an opportunity arises in the future that requires much larger arrays and/or higher serial data rates, we have a design solution in hand and we can easily upgrade the hardware to meet the requirement.

Lessons Learned

There were no major breakthroughs or discoveries in this task, but then, the scope of this task was more of an engineering design and development effort than a research project. Most of the “Lessons Learned” would fall under the category of project management.

This project required software development for an embedded, real-time, distributed processing system using multiple parallel processors. This is always a challenging task for the industry as a whole, especially for a young organization with many personnel new to the problem. From our experience we have learned that improvements in two areas could dramatically enhance the process and outcome of projects such as this. We list the two areas we will address in future projects:

- 1) Accelerate the hardware development of digital/programmable boards as much as possible, but not to the extent that the incidence of design errors and oversights increases. We found that traditional prototyping is unnecessary and impractical for high pin count digital circuits such as those we designed. In all cases we went straight from schematic to board layout with very few errors. In fact, for the System Processing Module (CCP and MTM) as well as the CDRC we had very little rework or “fixes.” In some cases we would even recommend going ahead with a board layout for a circuit that is not even fully complete, knowing that one will give the design a second “spin” later on to include the final design. This would have been useful in our case with the CCP where final details of the A and B interprocessor links were not fully resolved for several weeks after the rest of the circuit was fairly well defined. The main point is to get hardware built as

early as possible so the software development team has a real target system to work with, even if slightly incomplete in terms of features.

- 2) Structure the software development very much along the lines of hardware development where there are built-in mechanisms that clearly define the status of the effort. This is easier said than done, but from our experience the very free form nature of software development can lead to a situations where it is difficult to gauge the status of the project. While it is not our intent to digress into a treatise on software development project management methods, the paradigm we will be working toward in future efforts of this sort is illustrated below:

<u>Hardware Development</u>	<u>Process</u>	<u>Software Development</u>
block diagrams	conceptual design	bubble charts, flow charts, etc.
component selection	bottom-up design	define low level drivers
schematic	top-down design	define operational requirements
layout	physical realization	create user/host interface
review layout	reality check	get user feedback/trial run
order parts	preparation	write software modules
assembly	put it all together	integrate & debug software
test	verification	test

Note that as with hardware, it may take more than one pass to “get it right.”

Conclusions and Recommendations

The hardware has proven to be extremely capable and reliable. We encountered very few design errors in any of the system level modules including SCP, MTM, CCP, and CDRC. As the system stands it may easily be scaled up to meet the requirements of segmented mirror arrays of several hundred segments. For arrays of 1,000 or more segments we would need to upgrade the system to the higher data rate FPGA, which was designed but not constructed under this contract. Since we do not foresee the requirement for such large segmented arrays in the near future, we are comfortable with our decision to implement the slower data rate system, which uses a 10 MHz serial data rate. This decision leads to lower power requirements and lower cost systems without limiting our ability to meet a wide range of system requirements for some time.

The software represents a dramatic step forward for segmented mirror systems. The graphical user interface is a welcome and needed development. This can be expected to make it much easier for new researchers to operate segmented mirror arrays such as the PAMELA Testbed and others.

At the conclusion of this contract the software still shows signs of immaturity and it is likely that the need for further refinements will become apparent with actual use. This is not at all uncommon for such complicated hardware/software systems.

Task 1.2 — Next Generation Segment Controller: WFS Upgrade

Under this subtask Blue Line demonstrated the low noise performance capabilities of quadrant PIN photodiode position detectors as a replacement to the Lateral Effect Diodes currently being used in the PAMELA wavefront sensor (WFS). Stellar objects were used to demonstrate the radiant sensitivity of these devices and to further quantify their signal to noise (S/N) performance during prototype testing. Finally Blue Line retrofitted PAMELA's existing 36 subaperture WFS with this new design. This portion of the final report details the work completed by Blue Line Engineering to meet the objectives outlined above

Design and Analysis

Detector Selection

The contract called for the testing of three quad photodiodes. After an extensive catalog search (manufacturers Hamamatsu, EG&G, UDT, and Centronic), only two quad photodiodes were found having superior noise equivalent power (NEP) performance specifications. These photodiodes were the Hamamatsu S4349 with an NEP of $4.0e-15$ W/ $\sqrt{\text{Hz}}$ and the EG&G UV-140BQ-4 with an NEP of $7.0e-15$ W/ $\sqrt{\text{Hz}}$. Consequently these were the only quad photodiodes tested. The other manufacturers' products were at least a factor of 10 worse in their NEP. For comparison UDT's DLS10, the Lateral Effect Diode used in PAMELA, has an NEP of $1.0e-12$ W/ $\sqrt{\text{Hz}}$. Quad avalanche photodiodes (APD's) as well as miniature multi-anode photomultiplier tubes (PMT's) cost upwards of a \$1,000 just for the detector and were deemed too costly for this project.

It is interesting to compare the performance of these devices with that of a "noiseless" detector whose effective NEP is flux dependent and is set by the fundamental limit of photon statistics. The NEP of such a device operating at a Quantum Efficiency (Q.E.) of 60% and at a central wavelength of $0.7 \mu\text{m}$ (these parameters are similar to that of the quad photodiodes) is given by:

$$\text{NEP} = 4.1e-10 F^{1/2} \text{ W}/\sqrt{\text{Hz}} \quad . \quad [\text{Equation 1}]$$

where F is the incident flux in Watts. The flux for a zero magnitude star given the collecting area of a 7 cm hexagonal segment and assuming a spectral bandpass of $0.5 \mu\text{m}$ centered at $0.7 \mu\text{m}$ is roughly 42 pW. At this flux level, the NEP of a "noiseless" detector is $2.7e-15$ W/ $\sqrt{\text{Hz}}$. This value is only slightly lower than the NEP of the quad detectors. Therefore the quad detectors can be nearly photon noise limited for sources zero magnitude or brighter. Factors of 10 to 100 improvement in the NEP of quad photodiodes is also possible by cooling the devices to $-60 \text{ }^\circ\text{C}$.

WFS Electronics Design

Despite the excellent NEP specifications of the selected photodiodes, this performance is difficult to reach using conventional transimpedance amplifiers because of the Johnson noise introduced by the circuit's feedback resistor. Feedback resistors in excess of $1 \text{ G}\Omega$ are required to attain the level of performance possible for the selected quad photodiodes at room temperature.

The actual circuit designed for this project employs 10 M Ω surface mounted feedback resistors with through holes provided for testing higher valued resistors at a later time.

We have estimated the expected rms noise voltage (V_{noise}) at the output of the first stage amplifier for a feedback resistance of 10 M Ω and a bandpass of 1 kHz. A zero magnitude source illumination of 14 pA was estimated using the following parameters:

Central Wavelength = 0.7 μm

Wavelength bandpass = .5 μm

QE of detector = 60%

Collecting Aperture Area = 42 cm² (7 cm flat-to-flat hexagonal segment)

System Transmission = 100%

Note: Light from zero magnitude source falls on a single pixel

We found that the largest contributing noise source for the two quad detectors tested is $I_j R_{fb}$. If the feedback resistance is upped to 1 M Ω , the NEP specification of the Hamamatsu S4349 should begin to show better performance. By comparing the theoretical S/N performance gains on a zero magnitude source for the quad photodiodes versus the LEDD detector used in PAMELA, we expected to achieve a factor of 30 improvement for the 10 M Ω feedback resistor and a factor of 200 improvement for the 1 G Ω feedback resistor.

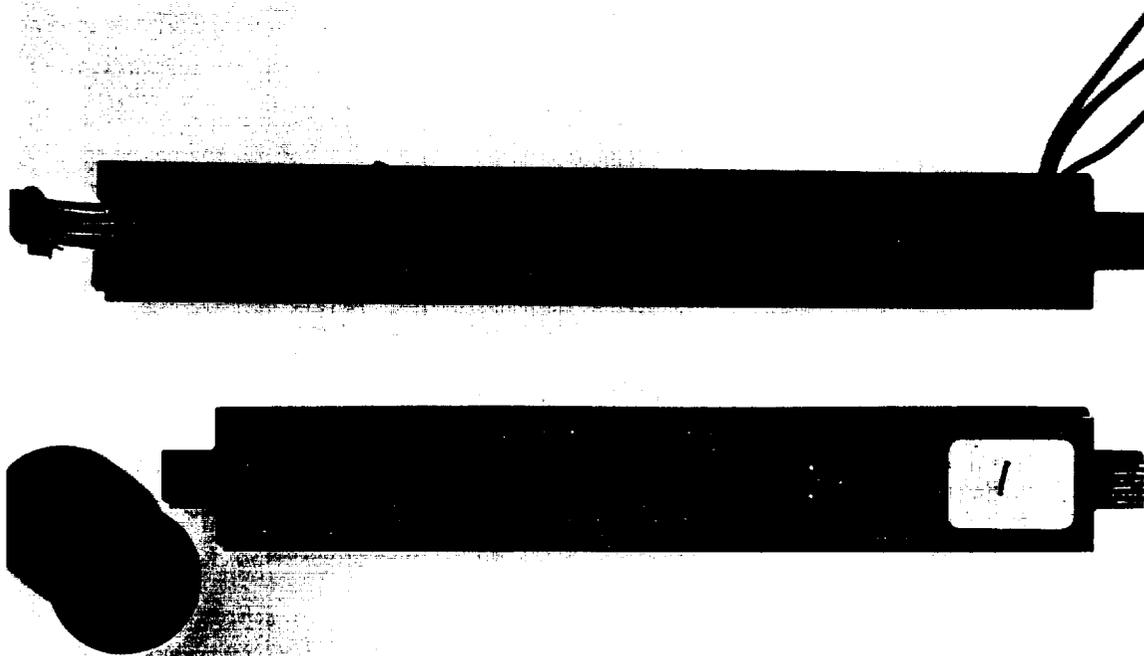


Figure 7: WFS detector electronics: Original WFS detector and circuit board (upper) and new replacement circuit board with PIN photodiode quad detector (lower).

The rest of the circuit provides the necessary signal conditioning and processing needed to deliver a usable signal to PAMELA's control system computer. The outputs of the transimpedance amplifiers are fed to a secondary gain and buffer stage and are then passed on to the op amps responsible for creating the difference and sum signals used to determine the position of a source. Our design has also been able to improve the performance of the WFS by providing a normalized gradient feature. This is accomplished using an analog divide circuit where the difference outputs are divided by the sum output. This allows for position measurements that are not affected by the intensity of the source and significantly reduce follow on signal processing.

Optical Design Considerations

PAMELA's existing WFS utilizes a 10x10 mm LEED detector and a set of fore optics with a 2.3 meter effective focal length (e.f.l.). This corresponds to an angular dynamic range (ADR) at the WFS of $4.3e-3$ radians. For a quad detector, the ADR is set by the angular spot size, provided its physical size is less than or equal to that of an individual pixel. The pixel size of the EG&G and Hamamatsu quad detectors are 1.5x1.5 mm and 1.3x1.3 mm respectively. To maintain the same ADR as the original WFS using a spot size equivalent to the pixel size, requires that the fore optics be adjusted to provide an e.f.l. of approximately 0.4 meters. In this configuration, the ADR can be narrowed considerably (up to a factor of 4) by focusing the spot. The extent to which this can be done is limited mechanically by the gap (.1 mm wide for the two quad detectors tested) separating individual pixels in the quad cell. The size of the spot is also limited fundamentally by the diffraction limit of the fore optics. For the 25 mm optic used in the PAMELA WFS this limit is $3.4e-5$ radians at the WFS.

To get diffraction limited images, the angular resolution requirements for the PAMELA WFS have been set at 400 nanoradians at the primary or 1 microradian at the WFS. To provide this resolution over the angular dynamic range requires S/N performance of 4300:1.

Test Results

Linearity Tests

A 1" tube was fitted with a 400 mm e.f.l. objective lens. The detector was placed near the focal plane of the objective and the tube assembly was mounted on the optical bench and supplied with a plane parallel light source generated by our ZYGO interferometer. A plane parallel mirror was used to control and vary the incident beam onto the wavefront sensor tube assembly.

For a basis of comparison, one of the PAMELA wavefront cells was placed in the optical train and the DIFF outputs of this board were monitored for angular position response. Keeping the y-axis fixed near the center of the detector, we checked the angular position response in the x-axis. The results of this test are shown in Figure 8. The output voltage of the DIFF output is plotted along the abscissa and the adjustable mirror's micrometer position in units μm is plotted along the ordinate. Each 10 μm step corresponds to a 170 μradian angular deviation at the WFS. As can be seen in Figure 8, the ADR of the PAMELA sensor is $3.0e-3$ radians. This is roughly 25% smaller than the target value of $4.3e-3$ radians noted above. The implied 3.3 meter e.f.l. for the optics used in this test cell is somewhat longer than the 2.4 meter e.f.l. described in the PAMELA documentation. The first two test runs were done before efforts were made to keep stray radiation sources off the detector. Tests runs #3-#5 are very repeatable as seen in Figure 8.

A similar analysis was done for the y-axis angular position sensitivity. The results of this test are shown in Figure 9. Again we see stable response for curves #3 and #4. Lastly the x-axis angular position response was checked as a function of different y positions. The results of this test are shown in Figure 10.

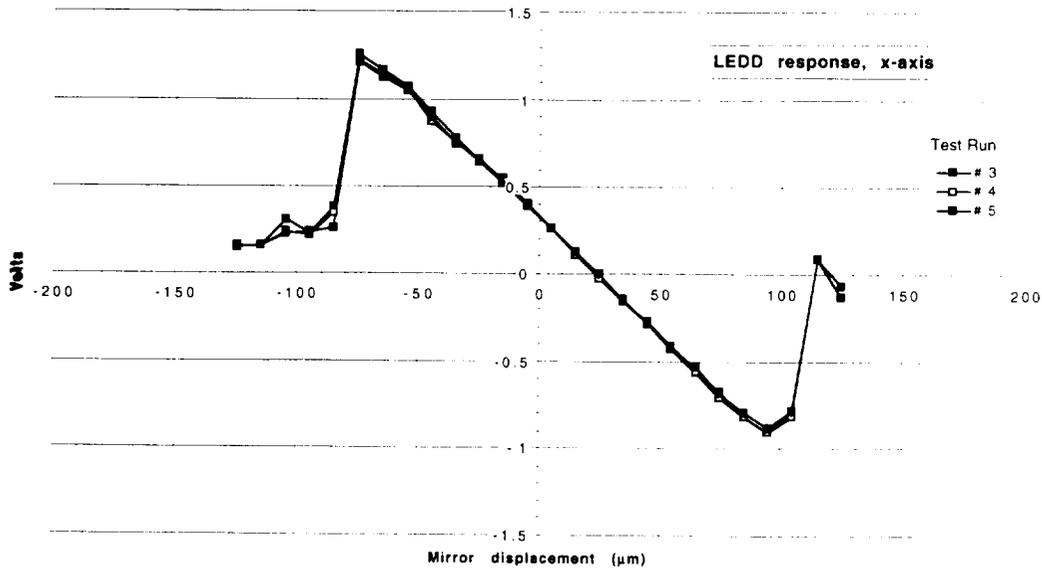


Figure 8: Response of original PAMELA WFS x-axis, lateral effect diode device.

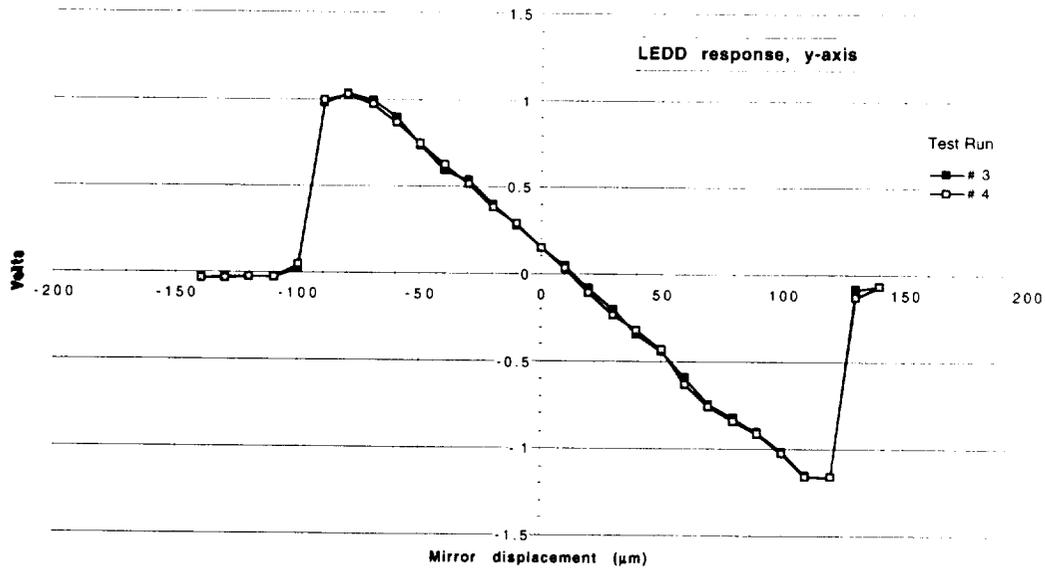


Figure 9: Response of original PAMELA WFS y-axis.

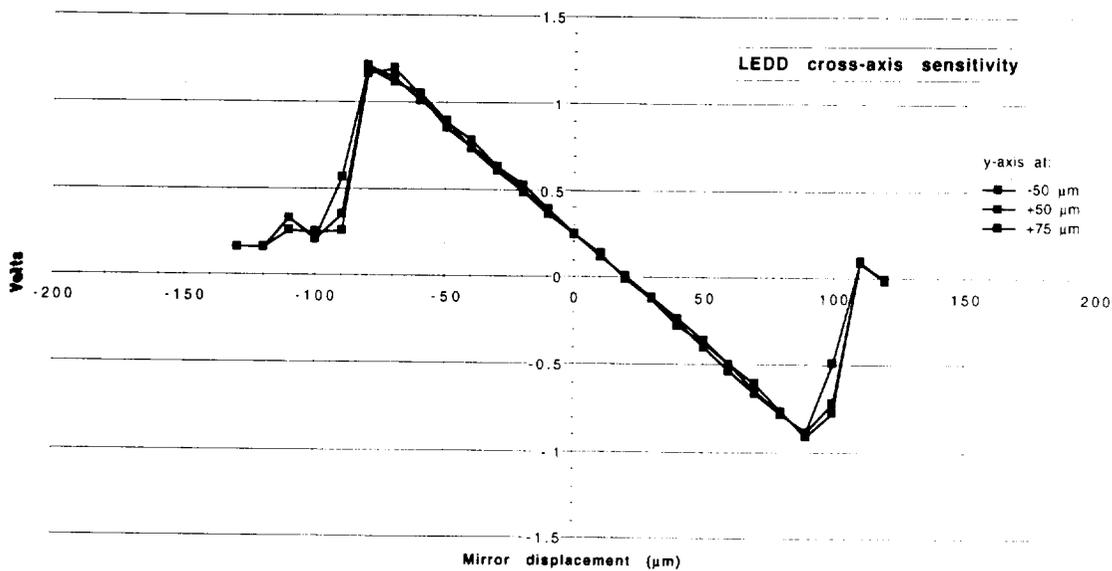


Figure 10: Cross-axis sensitivity test, original PAMELA WFS.

The original WFS was then replaced by the new prototype. The first board to be tested was one fitted with the Hamamatsu S4349 quad photodiode. This detector has 1.5mmx1.5mm detector elements. A neutral density filter of optical density of 2.0 was again used to keep the final stage outputs out of saturation. For the new prototype boards, we monitored both the DIFF outputs as well as the Normalized Gradient outputs. The results of the x-axis angular position response are shown in Figure 11 (DIFF output shown as V_d and Normalized Gradient output shown as V_n). The separation parameter refers to some arbitrary position of the wavefront board relative to the objective lens in centimeters. As shown later, this parameter describes the relative focus of the spot and therefore the slope of the angular position response.

An additional neutral density filter of optical density 0.5 was added to the beam and the x-axis angular position response was again monitored. The results of this test are shown in Figure 12. Note the identical behavior of the Normalized Gradient output for the two different light levels.

The y-axis angular position response was then checked. We noticed slight kink in the response curve near the middle of the range when plotted. We suspect this has something to do with the relatively small spot size used in this configuration and any inhomogeneities in the detector and/or optical set-up. The y-axis (G_v) angular position response as a function of two different x (G_u) positions is shown in Figure 13.

The y-axis angular position response was then monitored as a function of different focal positions. We found that the sharpest focus is achieved around a separation of 13 cm. The best match to PAMELA's WFS is seen at a separation of 10 cm. Three of the curves for separation 10, 11, and 12 cm are shown on a single graph in Figure 14.

The Hamamatsu prototype board was then replaced by a board fitted with the EG&G UV140 detector. This detector has 1.3mmx1.3mm pixels. The x-axis angular position response was then monitored with the results displayed in Figure 15. The separation parameter was then varied

from 10 to 12 cm and the results of this test are shown in Figure 16. These results compare well with those seen in Figure 14 for the Hamamatsu detector.

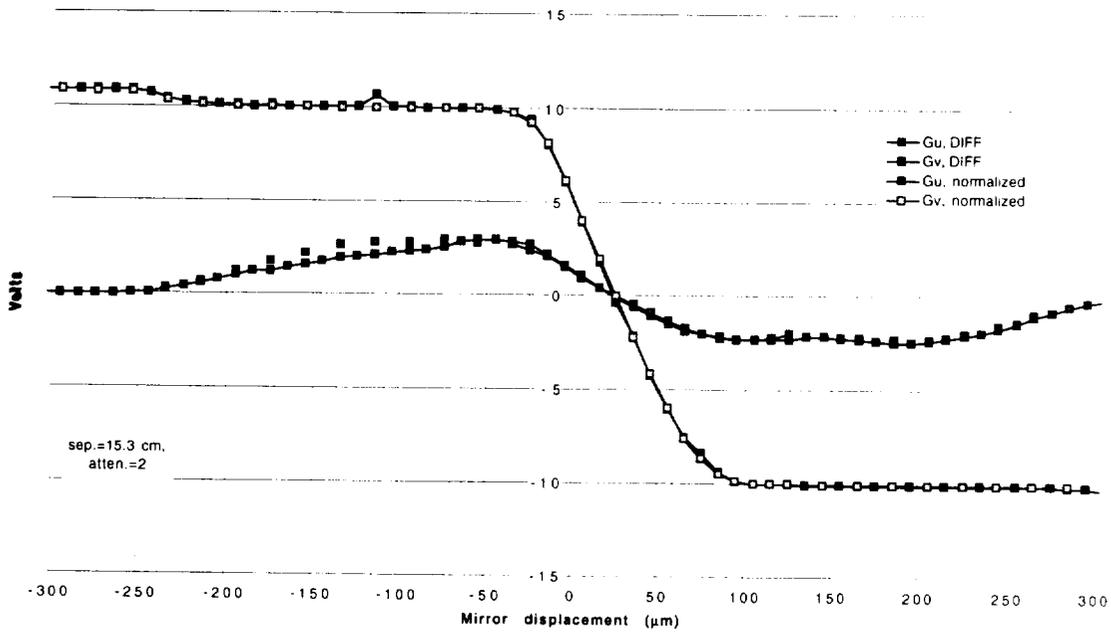


Figure 11: Response of upgraded WFS showing response of both x-axis (Gu) and y-axis (Gv), both differential and normalized outputs for Hamamatsu quad photodiodes.

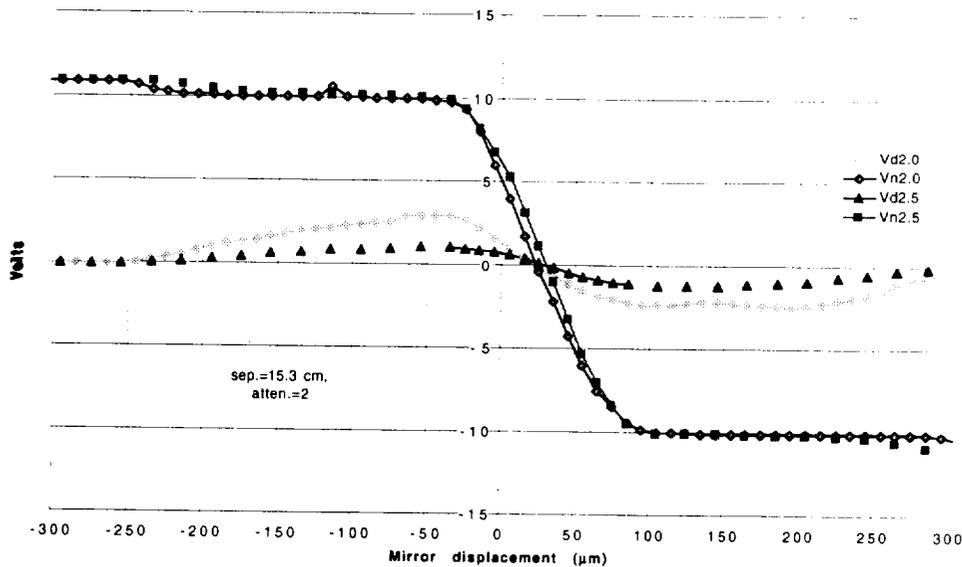


Figure 12: Response of upgraded WFS showing response of the x-axis (Gu) at two different illumination levels using the Hamamatsu detectors. The slight offset in the curves is probably due to the introduction of the neutral density filters into the optical path.

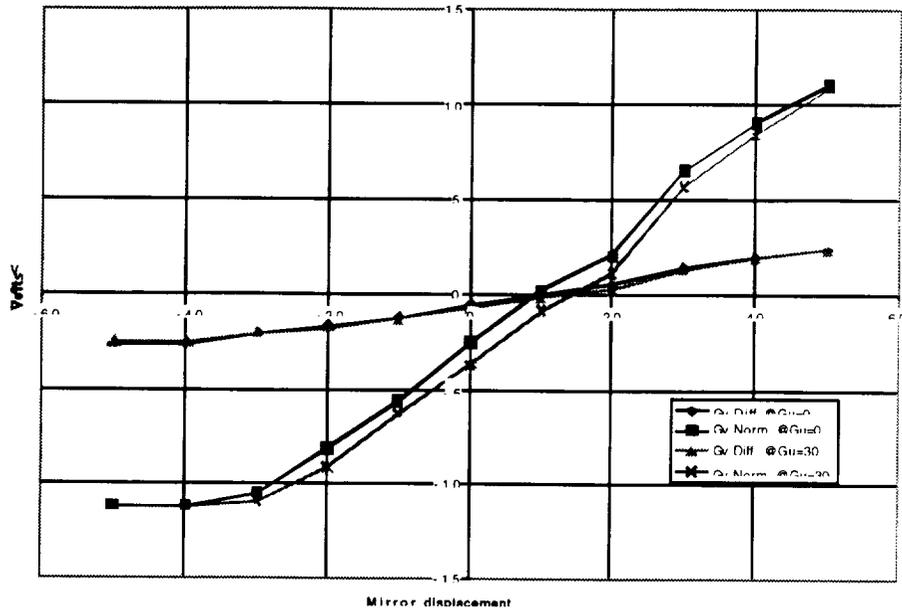


Figure 13: Gv response (y-axis) of Hamamatsu detectors at Gu=0 and Gu=30 μm.

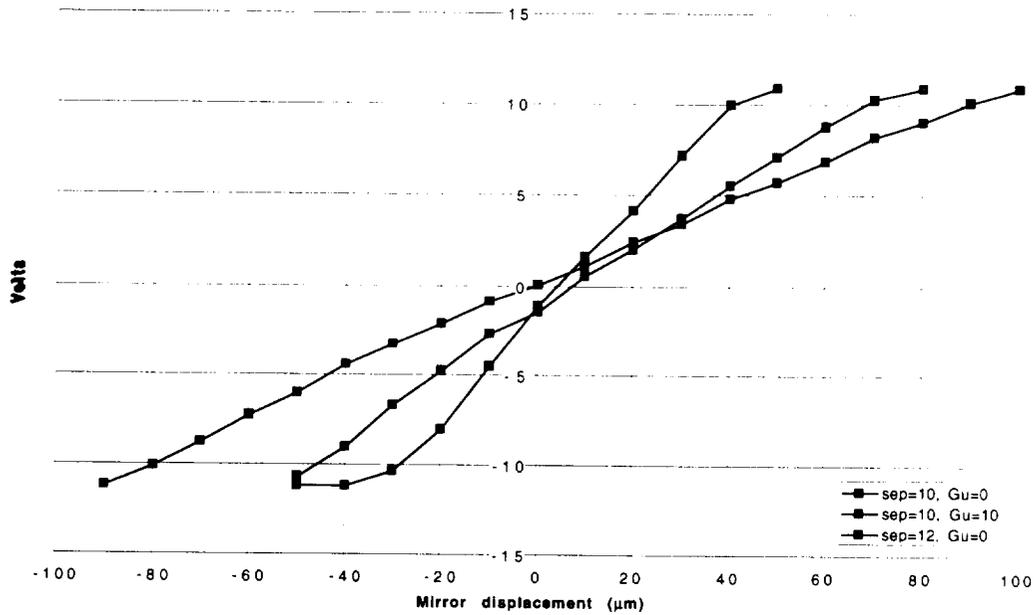


Figure 14: Gv response (y-axis) of Hamamatsu detectors at three different focus positions.

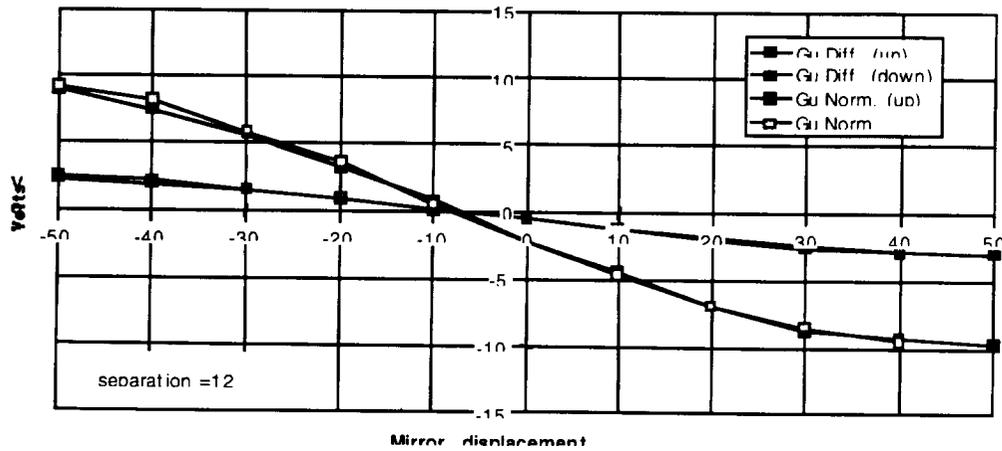


Figure 15: Response of EG&G detector with upgrade WFS electronics, both normalized and differential outputs plotted.

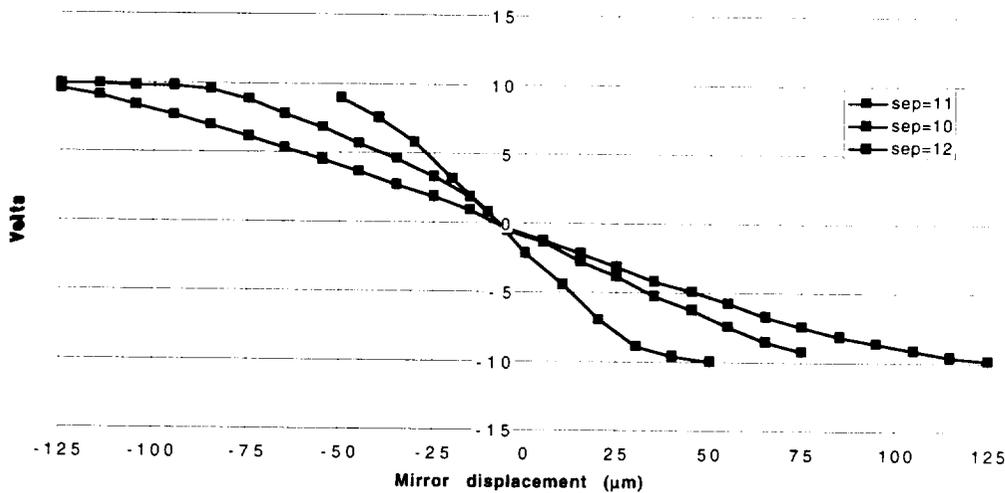


Figure 16: Response of EG&G at several different focal positions.

Signal to Noise Performance

Along with the linearity tests described above, we also measured the noise performance of the prototype boards along with the original wavefront sensor. At the output of the second gain stage where we have an additional gain of 10, we expect an rms noise voltage of .13 mV which implies a .65 mV peak to peak noise voltage. Using the differential scope input set to a 1000 Hz bandpass, we measured .5 mV peak to peak at this output. This value was measured for both the Hamamatsu and the EG&G detector. The noise voltage at the DIFF outputs were measured to be 1 mV peak to peak as expected since each of these outputs has four contributing inputs (noise sources add in quadrature).

These noise measurements were all taken with the detectors illuminated in the configuration described above (spot at the center of the quad cell). The noise voltage at the Normalized Gradient outputs was measured at 5 mV peak to peak. This was expected as there was an effective gain in this circuit of approximately 4 (V_d of ± 2.5 volts is elevated to V_n of ± 10 volts).

For comparison, the DIFF output noise voltage of the PAMELA wavefront sensor was measured to be 20 mV peak to peak. The signal to noise performance in identical illumination was $1.25 \text{ volts}/.020 \text{ volts} = 62$ for the PAMELA wavefront sensor and $2.5 \text{ volts}/.001 \text{ volts} = 2500$ for the Hamamatsu and the EG&G detectors. This is an increase of 40 in S/N performance. This compares nicely with the value of 30 predicted from theoretical considerations.

Stability Tests

It is extremely important from a control systems standpoint that the Normalized Gradient outputs be stable to some a fraction of a bit. The prototype board is designed to deliver a ± 10 volt signal at the Normalized Gradient outputs. Using a 12 bit Analog to Digital converter, this corresponds to a one bit accuracy of 5 mV.

To check stability of the prototype circuit, a test setup was used wherein a Light Emitting Diode (LED) coupled with a piece of diffusing material was used to provide a sufficiently constant source of illumination across the surface of the Hamamatsu quad photodiode. The intensity of the source (V_i , TP14) and the Normalized Gradient (V_n , TP12) were then monitored for stability. Results of several tests are shown in Table 1. Each test represents a slightly different set up where the relative position between the LED and the quad photodiode was varied. During each test, the source intensity was then adjusted by varying the dc voltage across the LED. As Table 1 shows, the Normalized Gradient output is stable to within ± 1 mV for source illuminations greater than ~ 1 volt. Below this value there is a migration away from some nominal value. This is attributed to stray radiation not associated with the LED onto the photodiode. Specifications for the AD734 Analog Multiplier and Divider component used in this circuit indicate that the circuit should be stable down to 0.1 volts.

Tests for longer term stability were also conducted by monitoring the Normalized Gradient output for a several hour period. This output was seen to vary less than ± 1 mV over this period. The setup was also checked for stability after it had been powered down and then brought back up. Again, stability on the order of ± 1 mV was noted with an equilibration time of ~ 15 minutes.

Stellar Calibration Tests

Site Selection and Performance Estimates

The Colorado College 16 inch $f/10$ telescope was chosen as the testbed for calibrating and verifying the performance of the prototype WFS board and the Hamamatsu and EG&G quad detectors. Two prototype boards each equipped with one of the two quad detectors tested, were fitted within a 1.25 inch aluminum tube so that it could be attached to the telescope using a standard 1.25 inch eyepiece mount.

Substituting a 16 inch aperture for the parameters discussed in section 2A, the estimated zero magnitude source current is 4.23-10 amps. Using a $10 \text{ M}\Omega$ feedback resistor and increasing the second stage gain to 100, the expected zero magnitude source voltage is .42 Volts.

The noise floor in this configuration is estimated to be a factor of 10 greater than that discussed in section 3 above due to the increase in the second stage gain. This should place it at 10 mV peak to peak at the DIFF outputs. Any additional noise can be attributed to tracking and seeing fluctuations on the source.

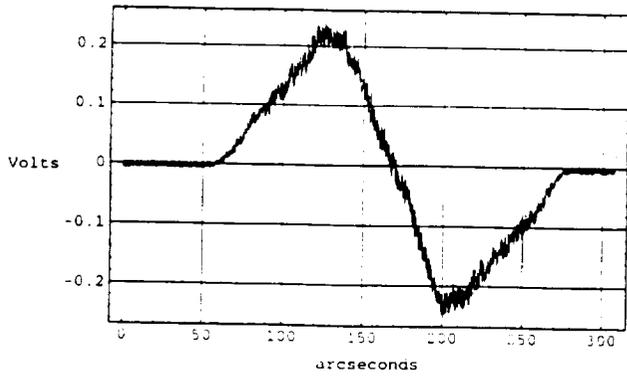
Position 1			Position 2		
VLED	VI	VN	VLED	VI	VN
3	0.2	0.065	3	0.136	0.098
4	0.614	0.098	4	0.528	0.153
5	1.345	0.103	5	0.988	0.162
6	2.25	0.103	6	1.723	0.165
7	3.54	0.103	7	2.647	0.166
8	4.77	0.103	8	3.6	0.166
			9	4.65	0.165
			10	5.71	0.165
Position 3			Position 4		
VLED	VI	VN	VLED	VI	VN
3	0.23	-0.061	2	0.172	-0.575
4	0.817	-0.025	3	1.616	-0.439
5	1.71	-0.019	3.5	3.972	-0.429
6	3.04	-0.017	4	7.07	-0.424
7	4.402	-0.017	4.5	10.06	-0.422
8	6.35	-0.018			
9	8.132	-0.019			

Table 1: Results of stability tests.

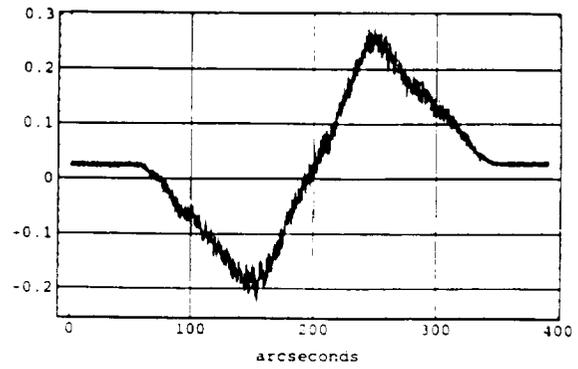
Field Tests

The zero magnitude source Alpha Lyrae (Vega), was used in the all the studies discussed in this section. Two types of measurements were recorded. One involved scanning the source across the quad detector at a constant rate using the telescope's guide control in either the Right Ascension (RA) or Declination (DEC) axis. The other involved fixing the source either on or off the detector. Data was collected at a 100 Hz rate for a 1 to 2 minute duration for any given measurement. The effective bandwidth of the measurements is set by the time constant of the transimpedance amplifier and its feedback network. Based on the feedback resistor and capacitor used in this circuit, this bandwidth is ~1,000 Hz.

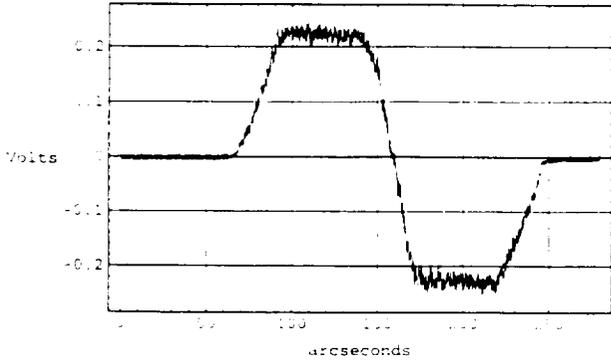
Scans were conducted for a variety of focal positions spaced 1 cm apart. These focal positions were referenced to the 1.25 inch tube assemblies and labeled A, B, C, D, and E. Figures 17a-h and 18a-h show the results of several scans taken for the two detectors in RA and DEC and at the different focal positions. The quad detectors were aligned by eye with the RA and DEC axes and the angular extent of the detectors was measured using the telescope's readout coordinates and were found to be 160 and 130 arc seconds for the Hamamatsu and EG&G detectors respectively. This compares well with the values of 155 and 134 arc seconds calculated using the telescope and detector parameters noted above.



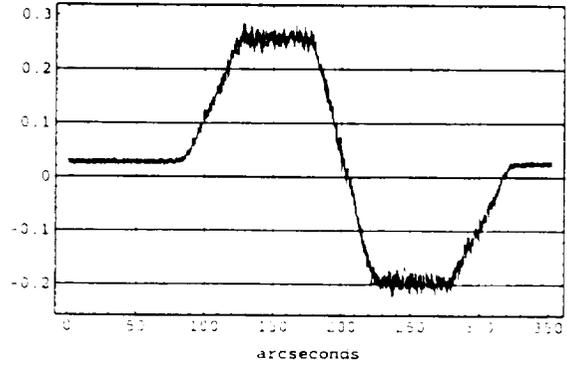
a) HAMAMATSU, Position A, Declination



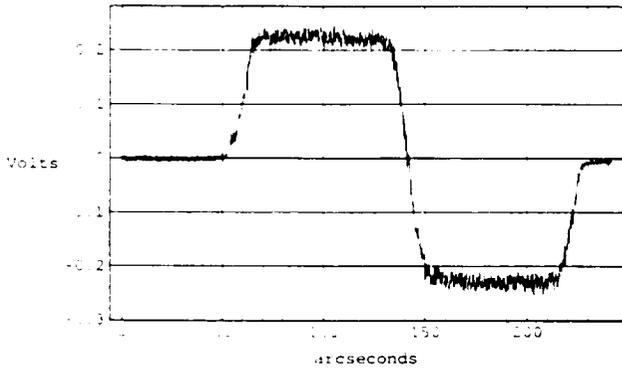
b) HAMAMATSU, Position A, Right Ascension



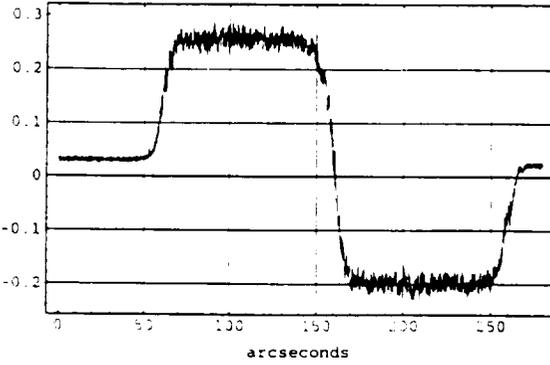
c) HAMAMATSU, Position B, Declination



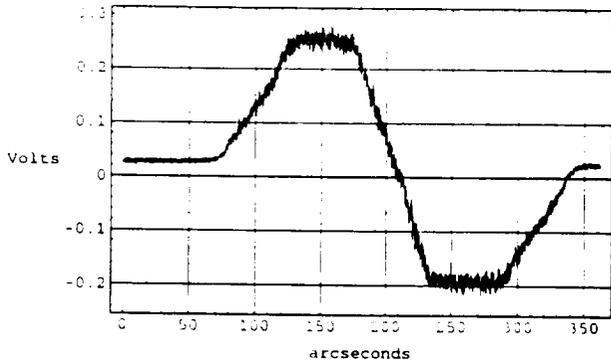
d) HAMAMATSU, Position B, Right Ascension



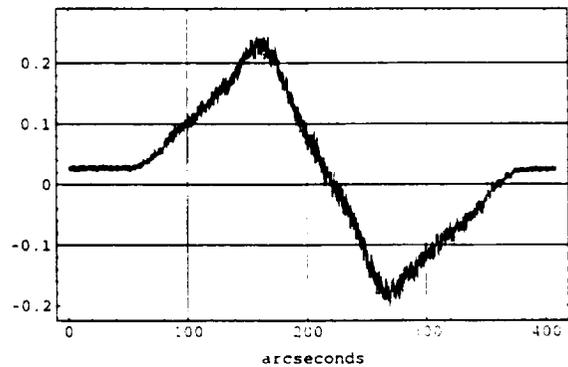
e) HAMAMATSU, Position C, Declination



f) HAMAMATSU, Position C, Right Ascension

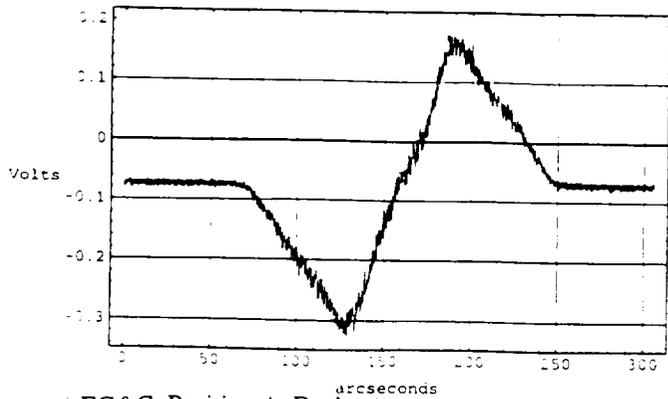


g) HAMAMATSU, Position D, Declination

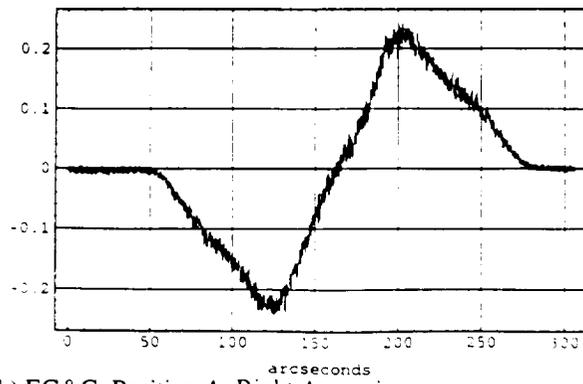


h) HAMAMATSU, Position D, Right Ascension

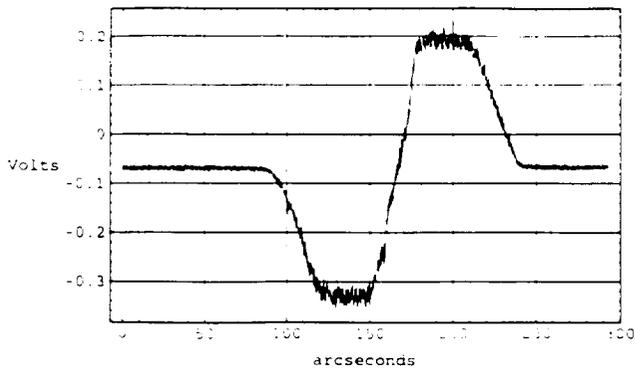
Figure 17a-h: Scan data for HAMAMATSU detectors at different focal listed in Table .



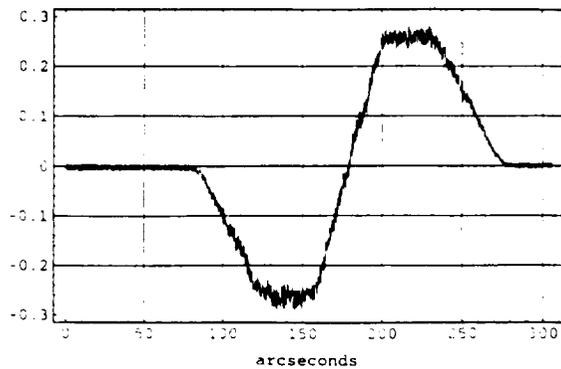
a) EG&G, Position A, Declination



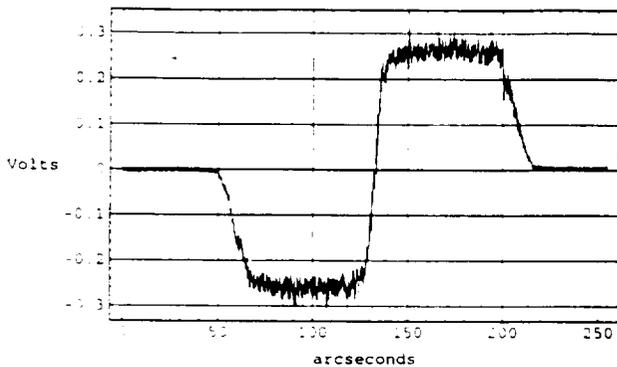
b) EG&G, Position A, Right Ascension



c) EG&G, Position B, Declination



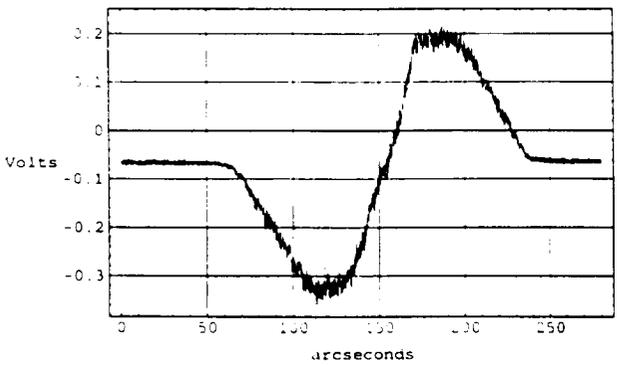
d) EG&G, Position B, Right Ascension



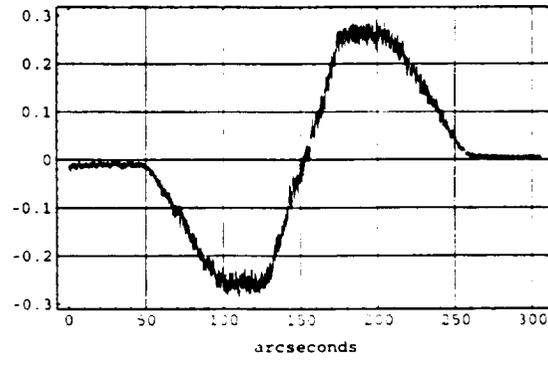
e) EG&G, Position C, Declination



f) EG&G, Position C, Right Ascension

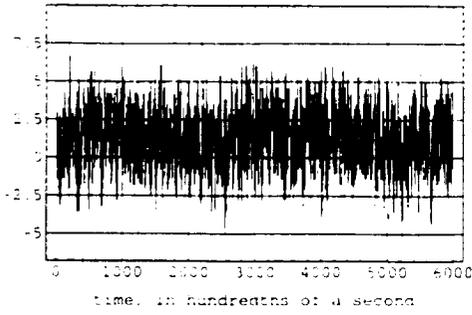


g) EG&G, Position D, Declination

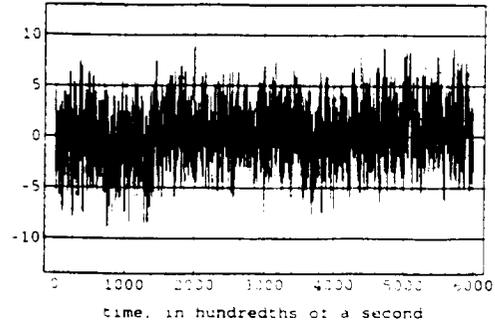


h) EG&G, Position D, Right Ascension

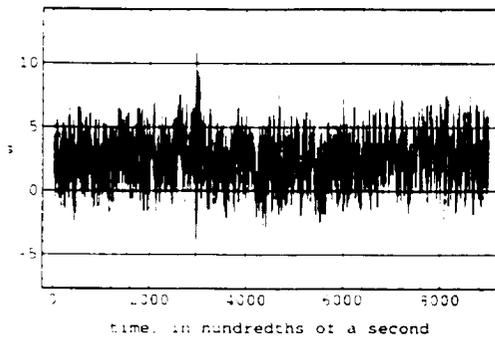
Figure 18a-h: Scan data for EG&G detectors at different focal listed in Table .



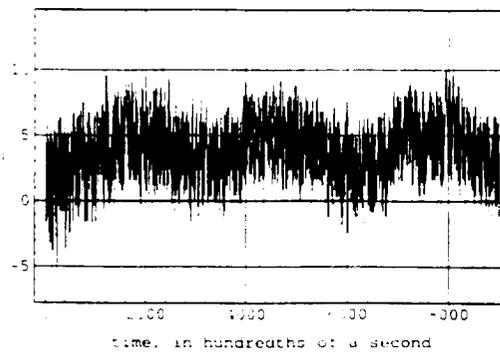
a) Hamamatsu, Position A, Declination



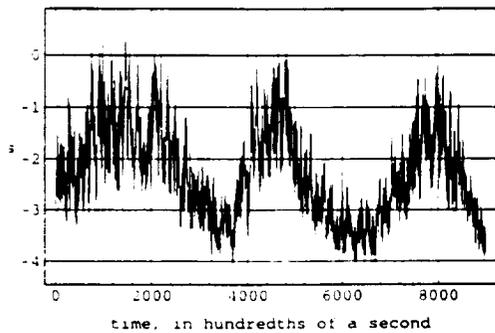
b) Hamamatsu, Position A, Right Ascension



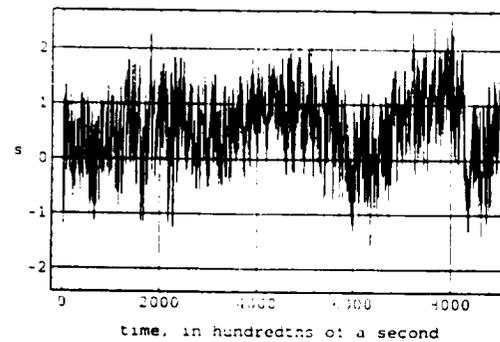
c) EG&G, Position A, Declination



d) EG&G, Position A, Right Ascension



e) EG&G, Position C, Declination



f) EG&G, Position C, Right Ascension

Figure 19a-f: Stellar centroid histograms for Hamamatsu and EG&G detectors at different focal positions.

The scanning measurements were used to calculate the slope (in units of volts per arc second) of the linear region where the star transits the central portion of the quad cell. The slope values for the various scans plotted in Figures 17 and 18 are listed in Table 2. One will note that the best focus was achieved for focal position C for both detectors. One can see from the scans that when the star is off the detector, the noise floor is approximately ± 10 mV as predicted above.

Stationary measurement were also taken where the star was positioned at the center of the quad cell and monitored for tracking and seeing fluctuations. Using the conversion of volts to arc seconds derived from the scanning measurements, the angular fluctuations of the star's centroid as a function of time for several stationary measurements are plotted in Figures 19a-f. The measured signal's rms given in arc seconds is supplied with each figure. The rms noise deduced from the off source noise floor (± 10 mV Peak to Peak or ± 3.0 mV rms) is also given in units of arc seconds. One can see from the data the seeing and tracking fluctuations were quite varied throughout the night ranging from 1 to 3 arc seconds with an overall trend towards better conditions as the night went on. The data clearly shows some tracking errors (seen primarily in the RA data) at a periodicity of ~ 30 seconds and a peak to peak amplitude of ~ 3 arc seconds in the RA axis. The lower amplitude periodicity seen in the DEC axis is most likely due to misalignment of the quad cell axes with the RA and DEC axes. The effective S/N of these measurements is as anticipated better for the C position scans where the source is in better focus.

The computed centroid motion of approximately ± 1.0 arc seconds is consistent with the kind of "seeing" one might expect from this telescope. Much of the poor seeing is can be attributed to "dome seeing". The CC telescope is located on a warm campus building and the dome has very little in terms of ventilation. As mentioned above, a trend towards better seeing was noted as the night went on.

As one can see the scanning measurements, the source brightness was roughly .3 volts, 25% lower than the predicted value. This can easily be attributed to some of the system unknowns such as effective bandpass and atmospheric and telescope transmission. The S/N performance on a zero magnitude star for a 16 inch aperture is therefore $.3 \text{ V} / 3 \text{ mV} = 100$.

Hamamatsu			EG&G		
Position	Axis	Slope (v/arcs.)	Position	Axis	Slope (v/arcs.)
A	Declination	6.87E-03	A	Declination	7.88E-03
A	Right Ascension	4.94E-03	A	Right Ascension	6.08E-03
B	Declination	1.67E-02	B	Declination	1.85E-02
B	Right Ascension	1.02E-02	B	Right Ascension	1.20E-02
C	Declination	3.16E-02	C	Declination	6.07E-02
C	Right Ascension	3.18E-02	C	Right Ascension	5.70E-02
D	Right Ascension	7.25E-03	D	Declination	1.19E-02
E	Right Ascension	3.93E-03	D	Right Ascension	1.02E-02

Table 2: Summarized results of WFS detector sensitivity using stellar scan tests at The Colorado College.

Signal to Noise Requirements and Their Implications

As noted above, the S/N requirements of the PAMELA system are currently 4000:1 for a bandwidth of roughly 1000 Hz. The Signal to Noise Ratio of a "noiseless" detector can be derived from equation 1 and is given by:

$$S/N = 1.5e9 F^{1/2} f^{-1/2} \quad \text{[Equation 2]}$$

where f is the bandwidth of the system given in Hz. We find for S/N = 4000 and f = 1000 Hz that an incident flux of 7.1e-9 Watts is required to give this level of performance. This would require a -5.6 magnitude star and a detector whose NEP (see equation 1) is only slightly better than 3.5e-14 W/√Hz. With a 10 MΩ feedback resistor, both quad photodiodes have an effective NEP of 3.0e-14 W/√Hz. Therefore system performance would not improve by going to a higher feedback resistor.

WFS Upgrade

Based on the test results and the S/N considerations discussed above, we proceeded to refit the existing 36 subaperture WFS with the prototype design without need for further modification. The boards were designed to fit in the same physical space as the original board and to accept the same connector. The only electrical modifications required were to provide ±12 Volts instead of ±5 Volts to the WFS boards, to provide some 5 Volt regulation for a few of the logic chips on PAMELA's WFS distribution tower electronics, and to modify the Wavefront Digital Interface (WFDI) boards to accept signals of ± 10 Volts. Some modifications of the software were required to allow for the normalized gradient. The optical configuration was also modified to provide an effective focal length of roughly 0.4 meters instead of the 2.4 meters originally used.

Work on the fabrication of 36 replacement boards for PAMELA's WFS was begun on July 29, 1997. Adapter plugs were designed and fabricated from Delrin to mount the quad detectors in the same assembly as used previously for the LEDD detectors. These plugs also allow for ± 40 thousands of an inch vertical and horizontal adjustment of the detector element.

The boards were completed and ready for test on August 13, 1997. The boards were then tested individually using the PAMELA system electronics and computer with the necessary hardware and software changes discussed above having been made. All 36 boards were tested for gross functionality and were found to operate normally.

Two of boards were checked more thoroughly for their S/N performance. With the optical configuration set up to provide an angular dynamic range of ~4e-3 radians, the rms noise from the Normalized Gradient outputs was seen to be approximately ± 1 digital count (out of 4096) corresponding to ± 5e-3 Volts at the output of the voltage divider. As discussed earlier in this report, this is as expected from the new WFS electronics.

The in house tests were completed on August 18, 1997 and the new WFS along with the other PAMELA WFS electronics and hardware were packed and shipped to NASA's Marshall Space Flight Center (MSFC) on August 19, 1997.

Integration and Test at MSFC

Blue Line representatives Gregory Ames and Dimitri Klebe arrived at MSFC on August 22, 1997 for purposes of integrating and testing the new WFS electronics with the PAMELA telescope. After installing a new set of 0.4 meter e.f.l. lenses in the PAMELA lens block assembly, the WFS electronics and hardware were set up and installed on the PAMELA telescope optical bench. With the direction of NASA employee Jeff Lindner, the output beam from the WYCO was successfully coupled and aligned with the WFS optics.

The quad detectors were placed at a focal position yielding a spot size of approximately 1.5 millimeters (angular dynamic range of roughly $4.0e-3$ radians). By monitoring the Normalized Gradient Outputs, each of the 36 detectors were aligned to their electrical null positions which corresponded to aligning the centroid of the spot with the apex of the quad cell. This adjustment was accomplished by translating the detector adaptor plug around and securing it in position via three attachment screws when the detector was at its desired position. All 36 detectors were successfully adjusted in this fashion.

The WFS electronics were measured to consume a steady state current of 1.6 amps at ± 12 Volts and operated at a temperature of ~ 48 °C with no shielding. Shielding was not required for 60 Hz suppression as it was in the laboratory tests conducted at Blue Line. We suspect that the grounded optics bench on which the WFS sat, provided adequate electrical shielding.

The next task was to make the necessary changes to the software to accommodate the Normalized Gradient inputs. Modifications were first performed on the program file **servoa.s**. The before and after listings of this code are attached with this document. Closed loop control of segments within group A was verified and identical changes were made for groups B, C, and D.

Once the software modifications were successfully implemented, we could monitor the S/N performance of the WFS. With the telescope taken out of the optical path via a reflecting flat, we verified that the angular dynamic range of the sensors to be $3.5e-3$ radians, close to the target value of $4.0e-3$ radians.

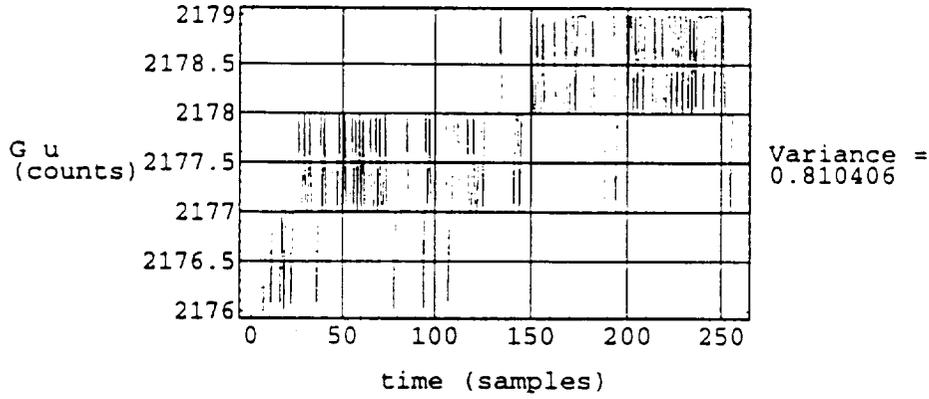
With the spot close to the null position and the detectors near full illumination (4096 counts), we noted the rms noise from the majority of Normalized Gradient outputs to be approximately ± 1 count. A sample of the data taken in counts for this sensor is plotted in Figure 20a-c.

We quickly discovered that some sensors were noisier than others and that this noise was associated with where the spot was on the detector. This noise problem was linked to the introduction of interference fringes at the entrance of the WFS optics and was not associated with any problems with the WFS electronics themselves. The outputs of the WFS were quite stable when the fringes were reduced.

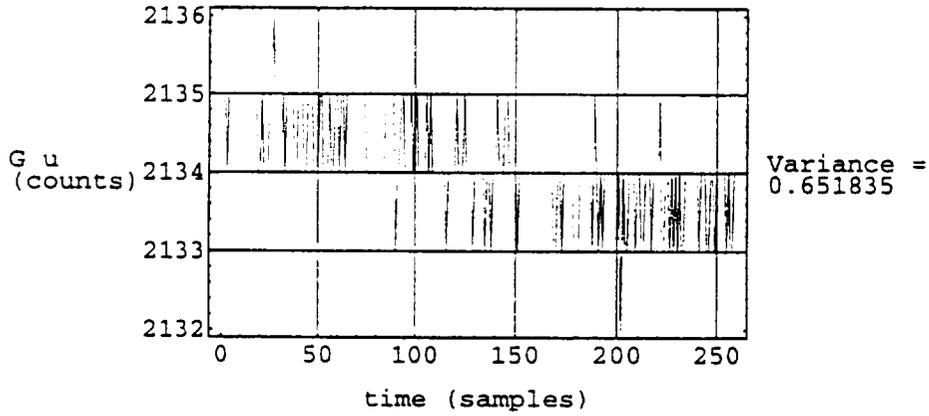
Photos of the installed WFS upgrade hardware are shown in Figure 21 a&b.

Figure 20a-c: Noise readings in counts, for Gu, Gv, and Ground.

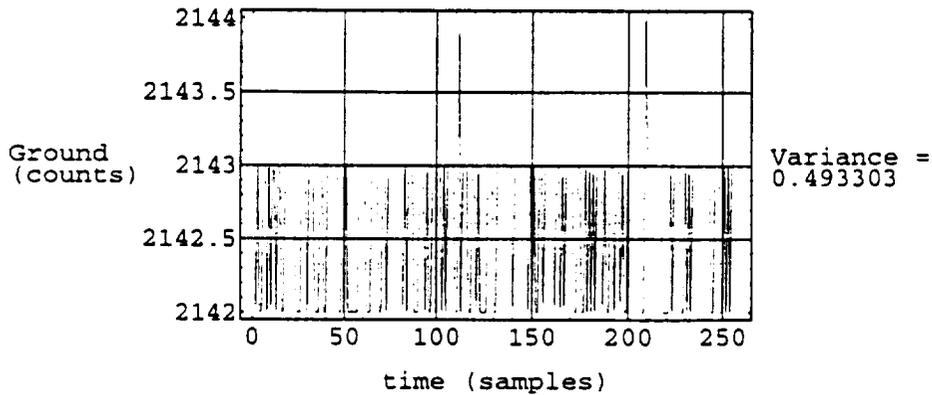
Gradient U Output
File C 80X 80Y



Gradient U Output
File C 80X 80Y



Ground Output
File C 80X 80Y



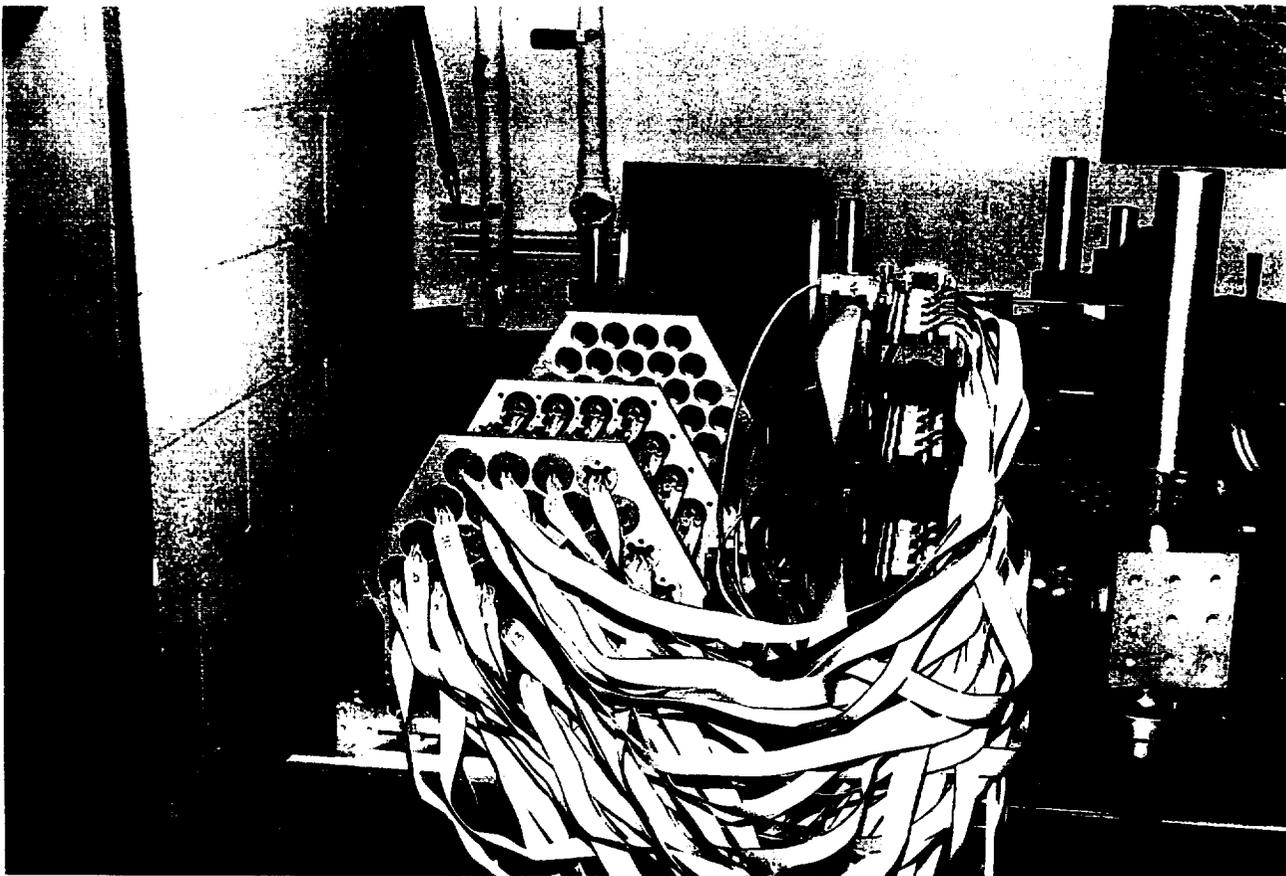
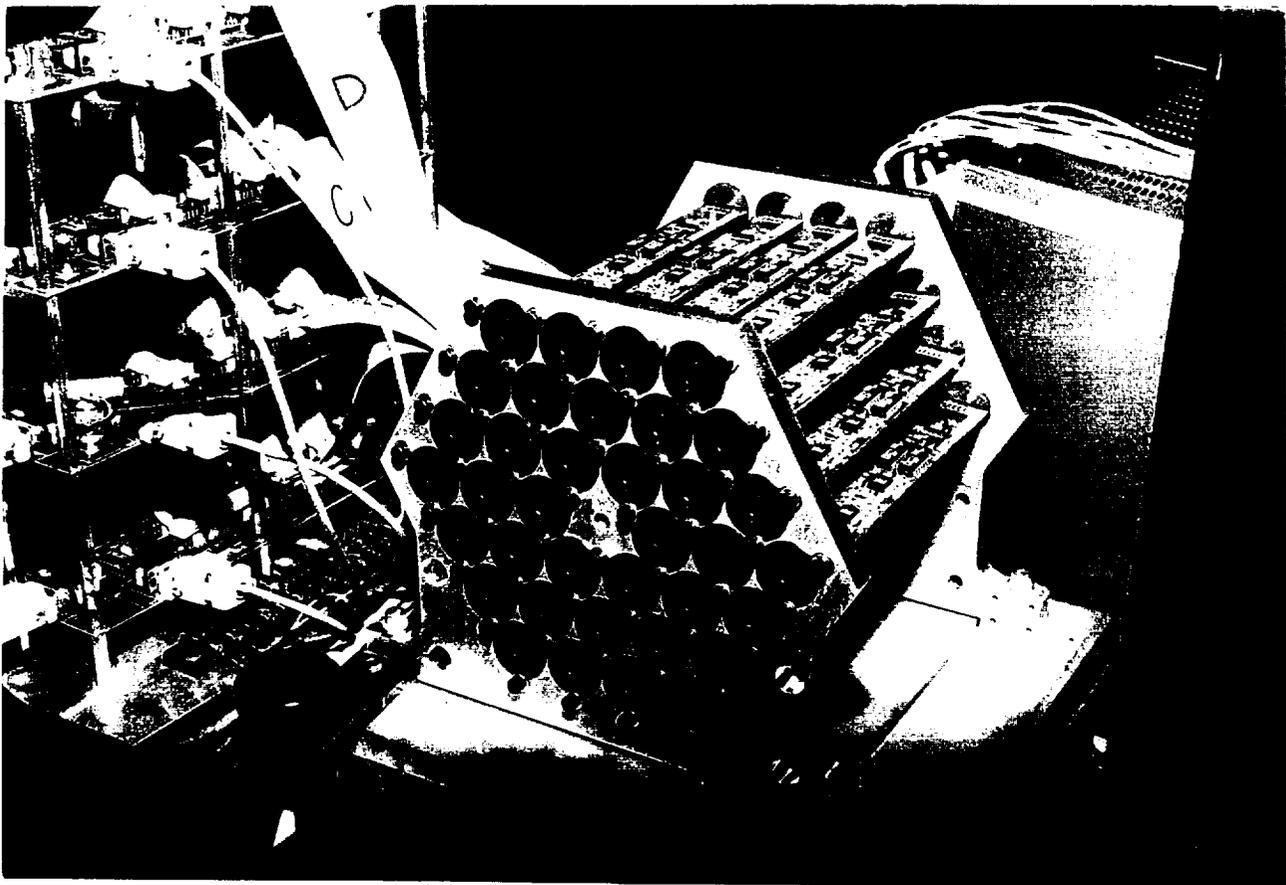


Figure 21: Upgraded WFS detectors installed on the PAMELA Testbed at MSFC; a) front view showing Delrin adjustment mounts; and b) rear view showing fore optics and cable harness.

Problems Encountered

The only real difficulty we encountered was that fairly early into the project it began to become clear to us that: a) photon statistics would limit the performance to fairly bright stellar objects no matter how perfect the detector was; and b) the best solution would be to completely redesign the WFS to use lots of small 64X64 pixel CCDs as super quad cells. The problem was that our objective was to achieve a significant improvement in performance on a very limited budget. There simply was not enough time or funding available to develop a new mini-CCD based WFS along with all the new readout electronics and digital interfaces that would be needed, not to mention the new optics that would be required.

Lessons Learned

One of the more interesting lessons we learned under this task was that the WFS sensitivity is significantly compromised by the need to maintain such a large dynamic range in the PAMELA testbed. The large angular dynamic range (ADR) is needed on PAMELA because the segment actuators have such a large throw and relatively unstable blind pointing capability. This means that the WFS must have a large capture range in order to be able to effectively close the tip/tilt loop reliably. This is why the PAMELA system has an ADR of approximately 4.3 milliradians at the WFS entrance pupil. It may be advantageous for future generations of segmented mirror systems of this type to take steps to dramatically reduce the open-loop variability or uncertainty in the optical alignment of the mirror segments. Perhaps this may be accomplished by implementing shorter throw actuators and/or co-located position sensors to improve the blind pointing accuracy of the segment when driven to preset actuator displacements.

Another finding was that with the analog normalization circuit included, as was done in this upgrade, one could adjust the sensitivity of the WFS in the transition region through null by varying the focus of the fore optics. This can be seen in Figures 14 & 16. Since the output voltage remains high or low beyond the transition region as long as the spot still falls on at least one of the quad cells, one can deduce which direction to drive the mirror actuators in order to get back into the linear transition region.

Conclusions and Recommendations

Integration and Test of the WFS upgrade was completed on August 28, 1997. The new WFS represents an improvement in performance of nearly 40:1 over its predecessor and provides the necessary capabilities for diffraction limited control of the 36 mirror segments. The next steps will be to rid the system of the unwanted interference effects so that this performance can be attained.

Task 1.3 — Next Generation Segment Controller: PAMELA Testbed Upgrade

This task was added to the SOW late in 1997 for the purpose of upgrading the PAMELA Testbed at MSFC to the latest generation of processing hardware and software for segmented mirror systems. The existing processing electronics was a one-of-a-kind prototype system that was becoming increasingly unreliable. The objective of this task was to replace the existing system processor, user interface, and control software. The telescope segment electronics and WFS electronics were to remain so the new processing system would need to interface with these existing subsystems. Photographs of existing hardware components can be seen in Figures 1&21.

Technical Discussion

Subsystem Interface Requirements

There are several important features of the existing processing system that needed to be taken into account. First and foremost is that the PAMELA system does not have any processing capability at the segment level. All closed-loop processing and compensation for actuator resonances must be performed at the system processing level. System processing is broken down to four equal Groups, each Group consisting of 9 of the 36 segments in the PAMELA Telescope. Actuator commands and edge sensor data are communicated between the segment electronics and DSP in serial format via a pair of differential digital data links for simultaneous transmission and reception of data at both ends. All of the segment electronics modules for a given Group are plugged into a custom motherboard just behind the primary mirror. A Segment Digital Interface board is included with each Group for communications between the DSP and segment electronics. A block diagram of the original PAMELA system is provided in Figures 22. Additional detail on the two main subsystems that must communicate with the new System Processor is shown in Figures 23 and 24.

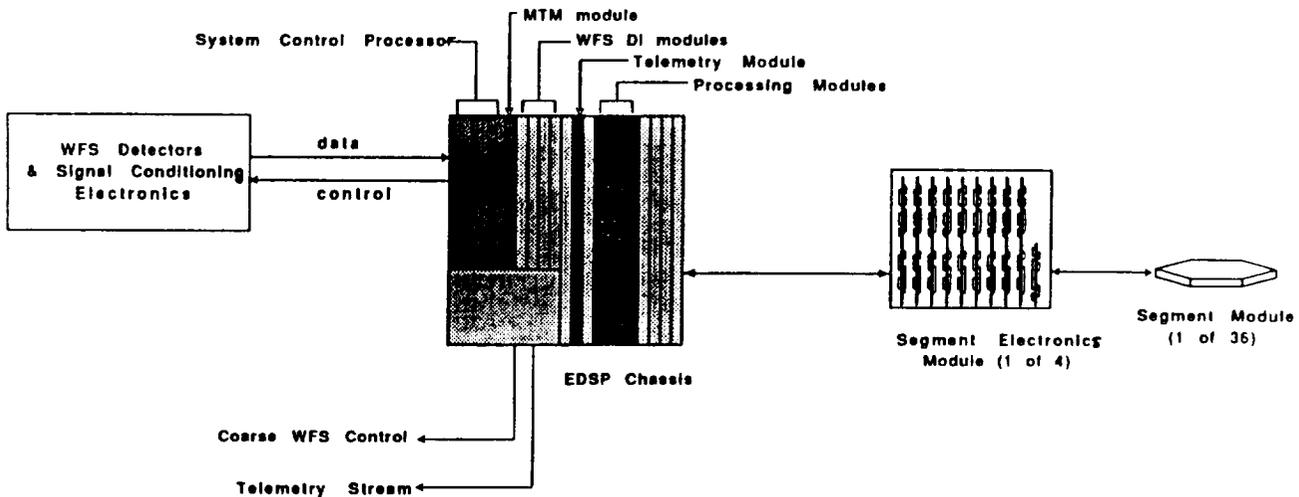


Figure 22: System block diagram for original PAMELA control system. The new System Processor must drop in and replace the large block in the middle, referred to as the EDSP Chassis.

Data Formats

The format of the data communications between subsystems of the original PAMELA Testbed are similar to the data formats used in Blue Line's new generation of system processing electronics. Both the old and new systems rely on frames of serial data formatted with a header field followed by 48 bit fields for each segment in the Group or Cluster. The main difference that we had to contend with in this upgrade project was that the old PAMELA processing system sent data as Least Significant Bit (LSB) first, which is uncommon in practice of digital communications. Also, it is more convenient to break down the 48-bit data fields for each segment into three 16-bit data words rather than two 24-bit words, as is done in the new generation of electronics. This eliminated the need to parse out the packed binary data at the CCP end of the communications lines.

Our solution was to modify the FPGA at the CCP module. One of the very nice features of the new generation of electronics is the use of these Field Programmable Gate Arrays (FPGA) at all communications nodes. The process involves a fair amount of engineering design and computer simulation work but once the design is debugged and ready to go all one needs to do is reprogram a small 8-pin configuration PROM and plug it in.

Clock Rate

The system clock rate on the original PAMELA System Processor was 4 MHz. The new generation of processing electronics uses a 10 MHz clock. In both cases the clock serves two functions. First it sets the bit rate for serial data communications. Second, and more importantly, the system clock is used by the edge sensor systems to drive and decode the inductive edge sensors. It is the second consideration which prevents one from just running a system at faster or slower clock speeds arbitrarily. To resolve this problem we simply substituted an 8 MHz crystal oscillator for the standard 20 MHz unit in the upgrade electronics. After dividing by 2, the System Clock signal provided by the MTM was then 4 MHz, which maintained compatibility with the existing subsystems on the PAMELA Testbed. Note that the Frame Rate did not need to be changed since it is set at 5 kHz in both systems, but we did need to change certain jumper settings in the MTM module to insure that the System Clock was properly divided to produce the correct frame rate.

Fiber Optic Interfaces

Blue Line's new System Processor uses fiberoptic serial data links to communicate with external modules. The original PAMELA system used differential line transceivers. In order to bridge this interface we built a fiber optic interface to the telescope and WFS subsystems. At the telescope end we built a small black box that accepts two fiber optic lines for each of the four Groups and also accepts a single fiber feed for system clock. The system clock is distributed to all four Groups internal to the black box. Coming out the back edge of the interface module we have four flat ribbon cables with connectors to mate with the original SDI boards for each Group in the PAMELA telescope. This module is shown in Figure 25.

In the case of the fiber interface to the WFS, we opted to build the function into the new WFS Digital Interface Chassis. We built the necessary circuits onto a 6U VME card that occupies the leftmost slot position in the chassis shown in Figure 26.

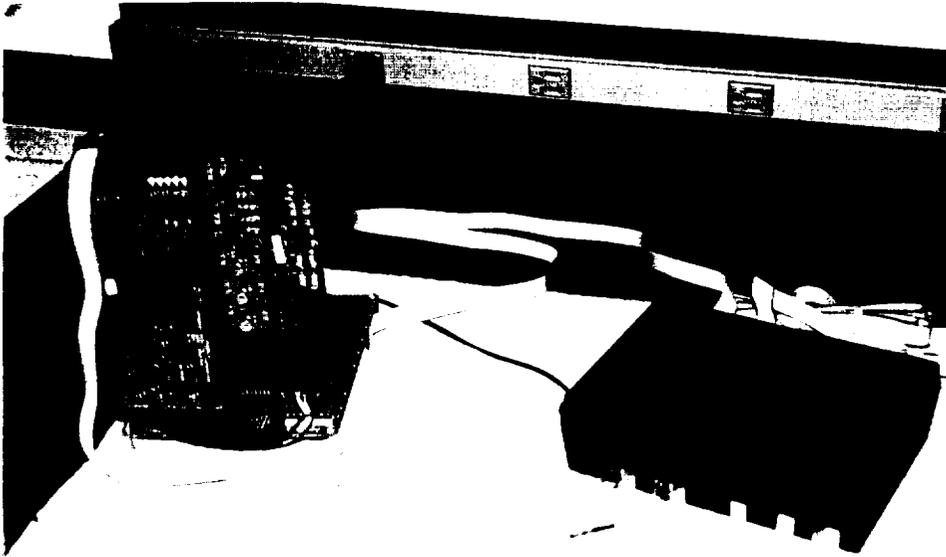


Figure 25: The fiber optics interface module, shown at the right of the photo, is used to convert fiber based signals to differential line digital signals for the SDI board, shown at left.

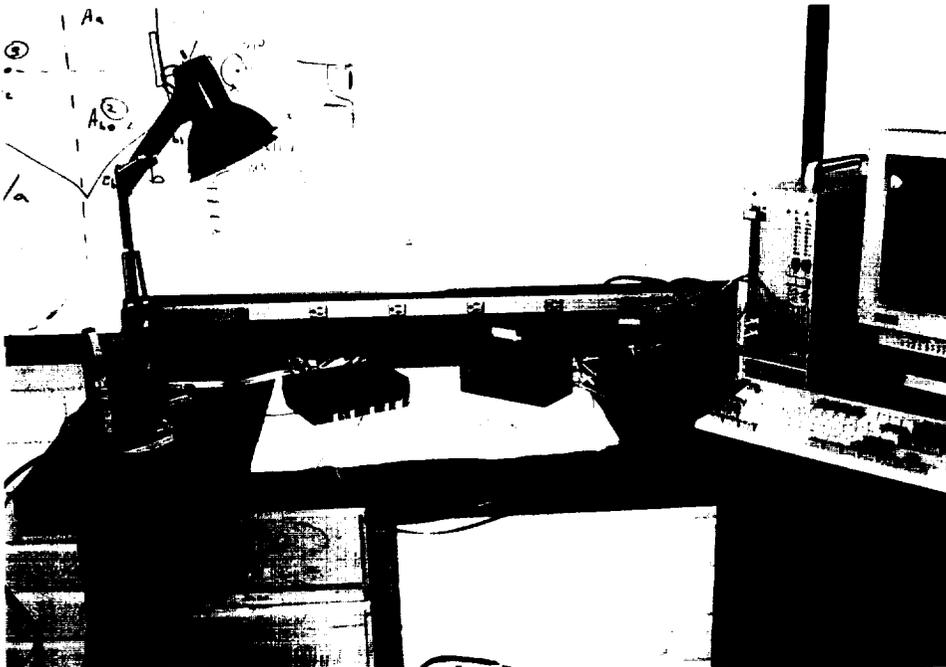


Figure 26: Test setup at Colorado Springs facility showing WFS Digital Interface chassis on the right, the processing modules (right of center), telescope fiber interface (left of center) and a subset of the PAMELA segment electronics used for testing purposes (far left)..

Customized User Interface For PAMELA

The user interface that was delivered with the original PAMELA Testbed was a menu style interface that required the use of keystrokes to operate. There are eight or nine different menu screens that are activated by pressing various combinations of the Shift, Alt, or Control keys. Each menu screen offered a text display of 12 different operations. To activate a particular function the operator had to press one of the function keys, which are usually located at the uppermost edge of standard keyboards. With experience, one could learn to perform most of the necessary operations with the testbed. But the interface was certainly clumsy and difficult to operate in a darkened laboratory. It certainly would not rank as a “user friendly” interface.

The new user interface is a Graphical User Interface (GUI), which we discussed briefly under Task 1.1, page 13, of this report. So the most striking feature of the new user interface is that it includes graphical features such as buttons, indicators, and intuitively obvious displays of the mirror array. Most operations are completed by using the mouse to point to a particular function or location and clicking on the mouse. A major benefit is that the operator no longer needed to refer to a “segment ID map” in order to control or interact with a given mirror segment in the array.

There are many other features that make this new generation of user interface a significant step forward for segmented mirror systems, too many in fact to attempt to list them all here. One significant difference between the old and new user interfaces that should be mentioned is that the old system was only useful when run on the PC type computer that was installed in the VME chassis. This is because the old system communicated with the DSPs via the VME backplane. The new system can be operated from almost any PC compatible computer, whether laptop or desktop. This is because the new system communicates with the DSPs via a serial data line between the PC and System Control Processor (SCP). In principle, any host or processor that could generate and interpret the serial data streams could serve in place of the PC and user interface. This would be especially useful if, for instance, PAMELA were ever to be flown on a shuttle mission.

Printouts of two of the screen displays of the new PAMELA interface are provided in Figures 27 & 28.

New Control Software

In addition to the task of tailoring the graphical user interface to the PAMELA system, the only other software task was to port the PAMELA control system over to the new hardware. The original closed-loop control algorithms were implemented on the prototype EDSP system developed by Kaman. The EDSP, which is an acronym for Extensible Digital Signal Processor, was based on AT&T’s DSP32 floating point processor. All original code had been written in the assembly language for the DSP32. Blue Line’s new generation of processing hardware is based on the Motorola 56301 series of 24 bit processors, which we also program in assembly language.

The control software is described in detail in the original PAMELA documentation. Additional detail on the new software is provided in the software manual delivered with the upgrade processor by Blue Line. The heart of the system is the control process that is performed once for all 9 segments in a Group for each frame of data. A block diagram for this control process is provided in Figure 29. One will note from this figure that there are two branches of incoming

data: WFS data (on the left), and edge sensor data (on the right). This data is coming into the CCP module via fiber optic lines and the resulting actuator commands (lower right) are sent out to the Segment Digital Interface via fiber optic lines as well. The SDI takes care of routing the data to the respective segment assigned to that group.

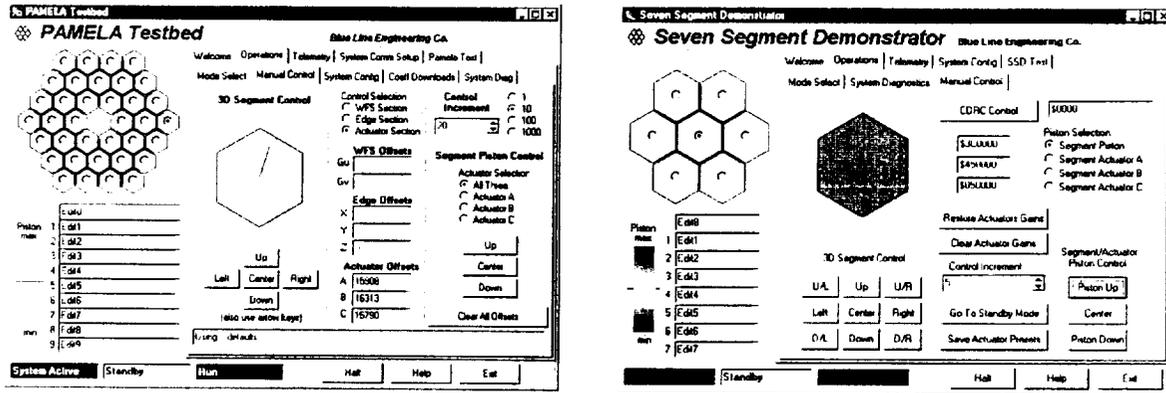


Figure 27: User interface screen displays for PAMELA Upgrade system (left) and initial user interface for SSD (right). These are one of several screens available to the operator. The color of the hex indicates the piston of the selected segment (see check boxes in hex display in upper left corner of each screen). The vector indicates tilt.

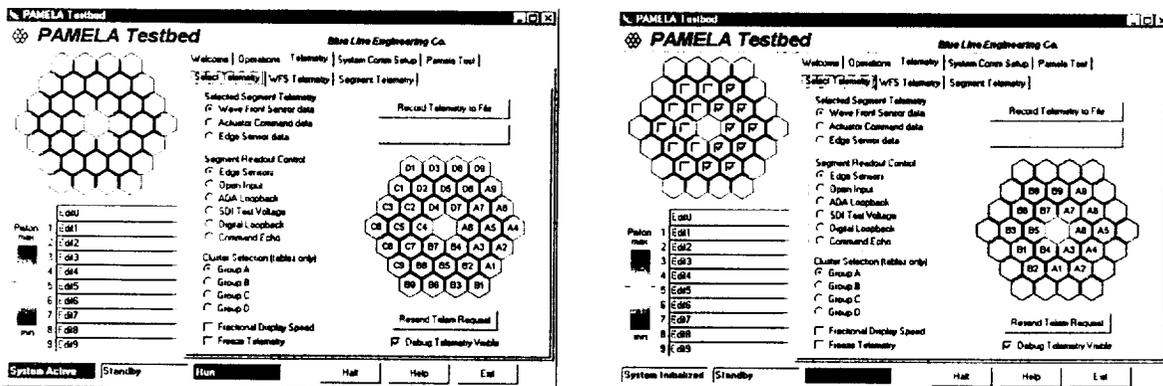


Figure 28: These screens show the two different segment mappings the system can accommodate. The one on the left is for the original 36 segment PAMELA system while the one on the right is for the more recent 18 segment .

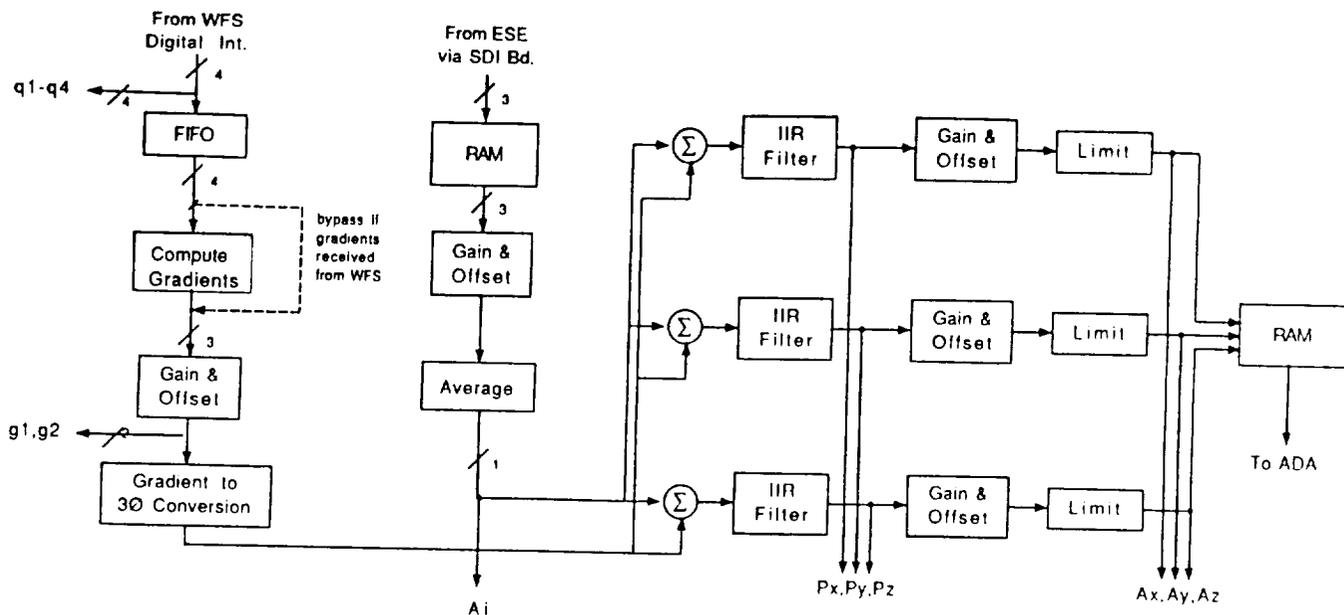


Figure 29: System block diagram for original PAMELA control system.

Problems Encountered

LSB vs. MSB First

The first problem we encountered was the fact that the serial data format used in the original PAMELA system was incompatible with the new system. As mentioned previously, this was due to the difference between sending serial data words in LSB vs. MSB first format. Initially we sought to keep the CCP standard so it could be interchanged with CCP modules in the SSD system. But this turned out to be almost impossible since we could not find the software for the FPGA on the Segment Digital Interface (SDI) board so we could not modify the system at that end. As it turned out this did not really matter since the PROMS that are used configure the CCPs would be different anyway, so they still wouldn't be directly interchangeable. We should note that the hardware is interchangeable but one must change both the small FPGA configuration PROM and the startup software EPROM to do so.

Once we settled on the correct course of action we did not have any particular difficulties in working around the problem. This helps underscore the power and flexibility that the use of these Field Programmable Gate Arrays (FPGA) add to digital systems. This new generation processing systems for segmented mirrors utilizes these devices at several strategic locations throughout the system.

Reconfiguration of PAMELA Mirror Array

The next real problem that we ran into was that the configuration of the PAMELA testbed changed from 36 to 18 segments. We had already completed the GUI interface based on the full 36 segment array when we discovered that NASA personnel had reconfigured the system to operate with only half of the segments due to efforts to get a number of the original mirrors refigured. As a result the entire assignment of a given mirrors segment to a given position in a particular Group had changed. This presents us problems at two different levels.

First, when the operator moves the mouse cursor to a particular hex in the segment array display and clicks the mouse button the system needs to be able to determine which of the four Groups that segment belongs to and which position (1 through 9) it is assigned to. This is

accomplished by means of some sort of mapping arrangement. Generally the segment assignment map does not change, but this occurrence helps illustrate the subtle difference between the user interface capabilities of a system to be used for research vs. one that is dedicated to an operational system.

This also presents a problem in terms of the graphical display the software must create. Do we provide two different array displays, one with 36 segments the other with 18? For now the solution is to present the operator with two choices on the System Initialization Screen: 18 Segment Configuration; and 36 Segment Configuration. The software then generates the proper array display. To add even more options one will need to get into the GUI software development environment and add these options since the GUI interface is a compiled application program.

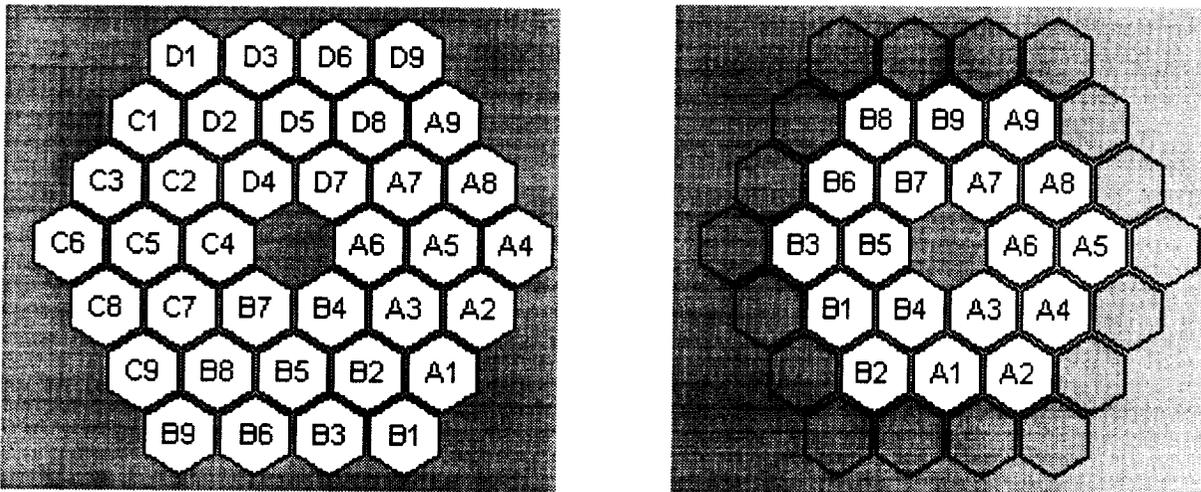


Figure 30: Segment array maps used for the original configuration of the PAMELA system (left) and the scaled down configuration currently in use (right). These maps provided a visual reference to the operator to indicate both segment ID number and Group Number assignments for a given segment in the primary mirror.

Lessons Learned

The only other problem we encountered during the upgrade of the PAMELA processing system was due to the difficulty of debugging the closed-loop process at our laboratory in Colorado Springs. While most of the functional operations of the hardware and software system could be effectively tested and debugged at our laboratory, the closed-loop operations really required access to the PAMELA testbed itself or an adequate simulation of the PAMELA testbed. Unfortunately we did not foresee the amount of difficulty we would encounter in this area. We have managed to work through most of the problems but the experience has led us to one of the biggest lessons of the project. In the future we will insure that similar projects provide for both the creation of a system simulator and more extensive periods of on-site integration and test activities.

Conclusions and Recommendations

A new processing system has been built, tested and delivered for the PAMELA Testbed facility at MSFC. This system represents a dramatic improvement over the first generation of processing electronics and software for the PAMELA Telescope. Hardware assembly and testing went very well in spite of some of the difficulties we encountered. This both a testimony to the solid design of the new generation of DSP hardware developed by Blue Line as well as an endorsement for the judicious use of FPGA technology in new designs.

Software development proved to be more of a challenge than originally expected. Overall the software is in good shape and provides the users with much greater capability than was ever possible with the original PAMELA system. But the lack of a proper simulator at Blue Line did hamper the debugging phase of the project, especially with regards to closed-loop processing. In the near future Blue Line expects to be utilizing this new processing system on two other projects, one of which is the NASA Phase II SBIR contract to construct the FAST telescope. Through these and other efforts, we expect to see a continuing maturation of the software at all levels.

Task 2.0 — Develop Concepts for Cluster Mounting Base

Technical Discussion

Concept Development

The role of the cluster base is especially critical in applications of segmented mirror technology where the mirror segments are on the order of 7 cm or smaller. The reason is that as the size of the segment gets smaller the relative density and mass of wires and cables becomes more of a problem and can ultimately dominate the total mass of the segmented array. The same applies to the mounting hardware. For example, even if the mass of the attachment and electrical interconnects totals no more than 2 grams, at 7 cm segment size this contributes almost .5 kg/m² to the areal density of the system. For a 3 cm mirror segment, the contribution jumps to just over 2.5 kg/m². Also, the difficulty of positioning the smaller mirrors increases with decreasing segment size. Yet another consideration to keep in mind is that one can easily support large 1 meter class mirror segments on an open truss but the only practical way to support arrays of 3 cm mirror segments is to provide a surface of some sort.

The original concept first proposed by Blue Line [1] was to integrate both electrical distribution and interconnection facilities along with mechanical mounting and attachment provisions into the structural support element referred to as the cluster support base. The cluster support base was envisioned to be as large as 1 to 1.5 m flat-to-flat, which is a size that facilitates integration and assembly of the full primary mirror if more than one cluster is required. Several years ago a mass budget was established for PAMELA type systems that allocated a 5 kg/m² areal mass budget for the cluster support structure (base). This number persists to this day as the target mass budget although little detailed design work has been done to support or alter this figure.

The objective of this subtask was to explore these concepts and produce a small conceptual demonstrator that could support an array of seven segments for the SSD. Initially the Cluster Base was to support an array of seven flat mirrors.

Design Issues

First and foremost, the cluster base must be a structural element that is rigid enough to support the cluster of segments without significant deformation under static or dynamic loads. As a rule of thumb we would set the maximum allowable surface error of the cluster base much less than the stroke of the segment actuator, ideally less than a few μm peak-to-valley. The cluster base must also be a low mass structure, our goal is less than the 5 kg/m², as noted above.

Since we are primarily interested in developing a concept for the cluster base that will support arrays of medium to small size mirror segments, we have concluded that the best approach is to include a near continuous front surface. This serves as the mechanical interface between the mirror segments and the cluster base. Open structures, such as webbed or truss type structures, were considered but discarded as likely to be too costly to implement and generally requiring a complete redesign for each new application. The approach we have selected for this development is to utilize a foam or honeycomb core with thin sheets of high tensile strength material laminated to both front and back surfaces. This is basically the same type of construction that is commonly used to build composite optical breadboards.

Since printed circuit boards are generally manufactured using laminated sheets of G-10 epoxy-glass material of various thicknesses, an obvious advantage of the honeycomb type construction

is that one can easily substitute a thin (1/32 inch or less) printed circuit board for the back skin. This is precisely the approach we took. One of the beauties of the system architecture developed under Task 1.1 is that it leads to a very simple electrical interface with each segment. Data is routed serially in a daisy-chain fashion. This allows the designer considerable freedom in laying out the serial data path linking the output of one segment to the input of the next. All other system resources (power, clock, and frame pulse) can be distributed in a starburst or tree type distribution network.

This leads to one other design consideration: whether to include any active electronics in the cluster base. Obviously once one has decided to layout a printed circuit board for distribution of electronic resources it is not too difficult to include a few provisions for some active circuitry as well. We chose not to do this for the conceptual prototypes we built. In some applications, particularly some aerospace applications, this may be very desirable. For example, the CDRC could be implemented on the Cluster Base or perhaps one could include local voltage regulation or EMI filters at the point of power supply delivery to the Cluster Base. The two main factors to be taken into account for such cases would be thermal dissipation and cost.

The cluster base must also include some sort of electrical interconnect between the distribution circuit and the local electronics associated with each mirror segment. Our initial concept was to put the distribution circuitry on the front side of the cluster base and implement some sort of pressure contact system whereby the segment would make electrical connections as it was attached to the cluster base. We chose not to pursue that approach at this time for two reasons. First, it would take considerably more engineering effort to develop a reliable interconnection mechanism than was budgeted for under this task. Second, in most cases the front surface of the cluster will need to be concave but at this time it is only practical to make flat printed circuit boards.

As it turned out, the most problematic design issue we faced in this effort was the method of mechanically attaching the mirror segments to the cluster base. The attachment method must provide for six degrees of adjustment. The main considerations are adjustments that allow the mirror to be set in tip/tilt and piston to a precision well within the correction capability of the actuators. For the current generations of active segments, this leads to an installation accuracy of $\pm 25 \mu\text{m}$ or better. The adjustment scheme must also allow one to set the gaps between segments to a similar level of accuracy since the nominal gap is $250 \mu\text{m} \pm 10\%$.

During this project we considered many different schemes, including magnetic and kinematic mounts, precision pin and hole patterns, and others (see Figure 31). The method we ended up using was a simple arrangement that utilized three screws with Belleville washers. As will be discussed later, this was less than satisfactory and mechanical attachment of mirror segments remains the #1 design issue to be addressed in future implementations of this concept.

Before leaving the issue of mechanical attachment, we should note that part of the challenge is to devise an attachment method that permits a significant amount of variation in as-built dimensions of the active segment assembly.

First Prototypes

The cluster base that was built and delivered as part of the SSD is a lightweight composite structure having two functions. First, it serves as a mechanical mounting platform for all components of the segmented mirror array. Second, it has a circuit board built into it that provides power, ground and signal distribution to each set of segment electronics. On the front

of the cluster base are the actuator assemblies, mirrors with edge sensors, and the actuator and edge sensor electronics. On the back are the segment DSP boards and the Cluster Data Router/Concentrator (CDRC).

The electrical signals distributed on the cluster base include +5vdc, -5vdc, ground, master clock (10 MHz), shift (derived from the frame sync), data in, and data out. This function is performed by a custom circuit board laminated to the back of the carbon fiber/honeycomb panels.

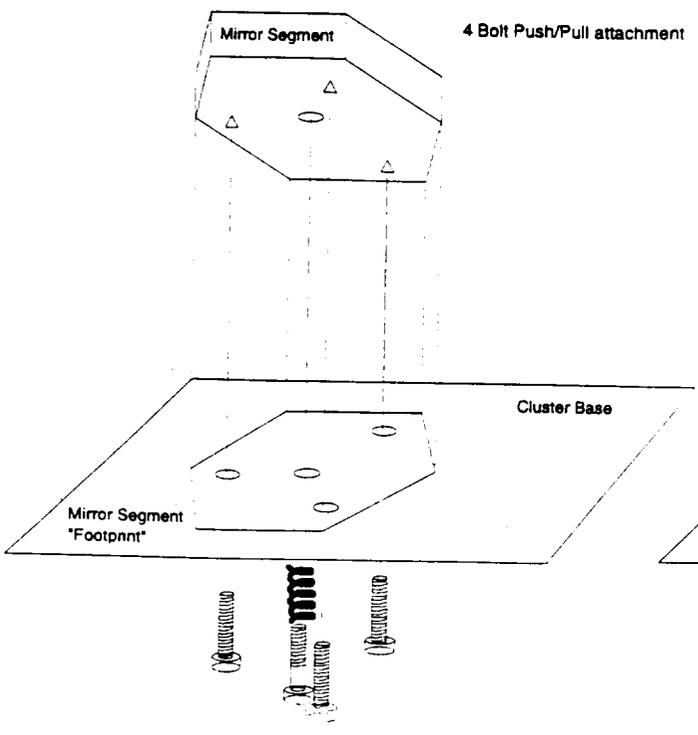
The flat cluster base must accommodate the 1 meter radius of curvature mirror segments. This is performed by the attachment of actuator mounting cups at appropriate angles and depths to allow the mirror surfaces to be approximately lined up prior to activation of the SSD control system. When operating, the SSD then forms the mirror segments into a continuous optical surface. The design also includes mounting points to allow the Cluster Base to be attached to an appropriate test fixture or bracket.

Two prototype cluster bases were actually constructed. The first had a balsawood core with a thin G-10 epoxy glass sheet laminated to the front surface and a double sided printed circuit board laminated to the back. The structure was very rigid and low mass but we felt that the use of the balsawood core would detract from the concept we were trying to illustrate with this prototype. Therefore a second unit was built using a graphite-epoxy laminate with Nomex honeycomb core.

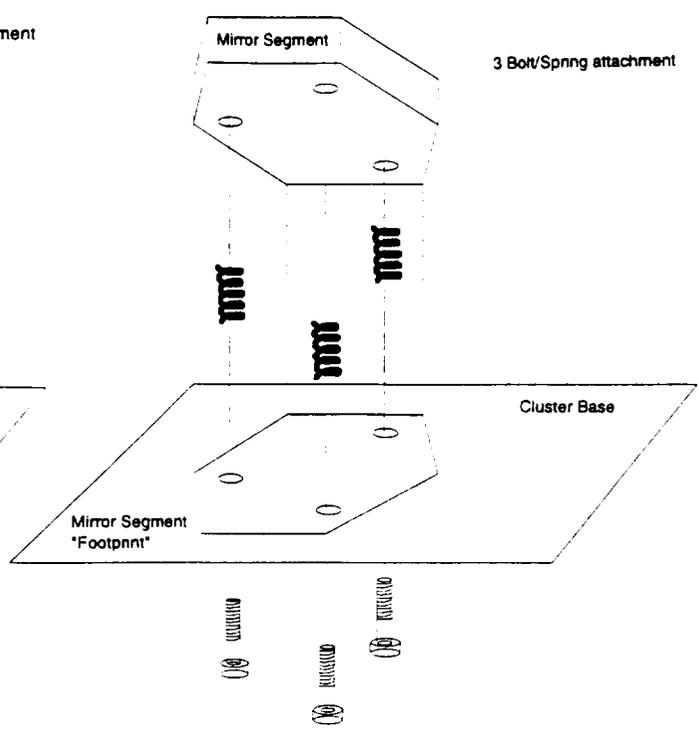
In the following pages we provide a number of sketches of some of the concepts we considered for both segment attachment and electrical interface (Figures 31 & 32). The actual prototypes incorporated the "3 Bolt/Spring" attachment concept and the "Flexible Pigtail" connection methods. These sketches are followed by a drawing of circuit board layout used on all prototypes (Figure 33)

In Figure 34 we provide a photograph of the rear of the balsawood Cluster Base with segment processing boards and a CDRC installed. Note that the array only requires the four fiber optic links (blue lines) for Clock, Frame Sync, Data-In, and Data-Out signals plus a power lead (gray cable) for ± 5 VDC and power common (or Ground). Note that the cross-hatch pattern serves as a ground plane.

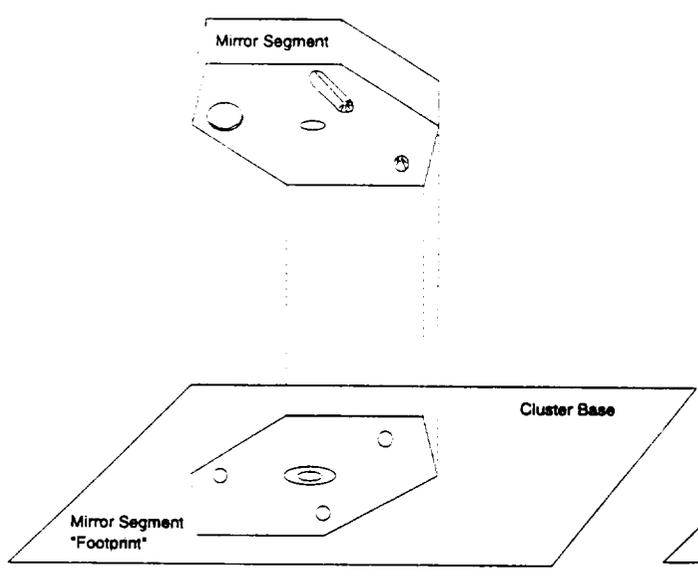
The next photograph (Figures 35) shows the front of the graphite-epoxy prototype with the aluminum segment attachment cups bonded in place. In Figure 35 one can also see the slots cut through the base structure to allow the flat flex cable to pass between the segment assembly on the front side to the segment processing board on the back side. While it is not evident from the photograph, the aluminum cups for the six segments that surround the central segment are all set at an angle relative to the cluster base. In the lower photo of Figure 35 we see the seven aluminum substrates (prior to final grinding and polishing operations) laying on top of the cluster base to illustrate the final orientation of the mirror array. This is the cluster base that was used in the SSD as shown previously in Figure 5.



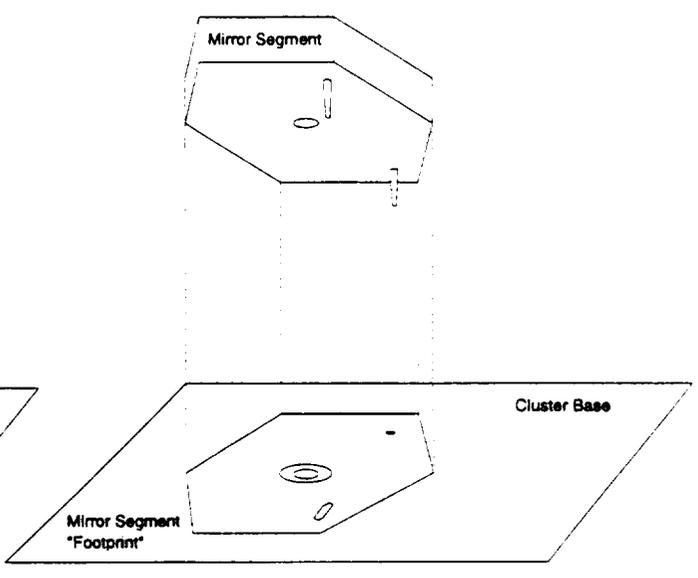
4 Bolt Push/Pull Attachment



3 Bolt, 3 Spring Attachment

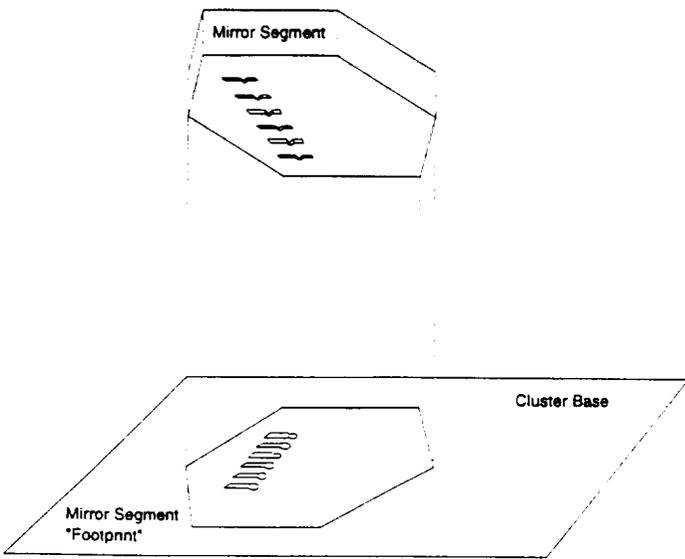


Cone/Groove/Flat Alignment,
Magnetic Attachment

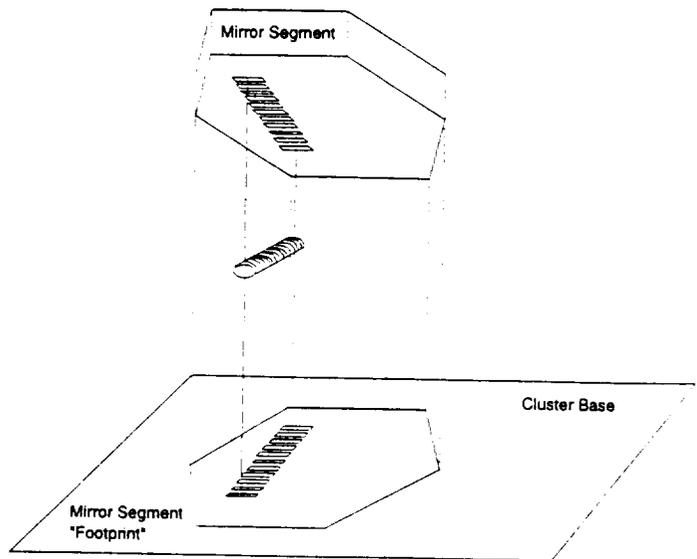


Dual Pin Alignment w. Slot,
Magnetic Attachment

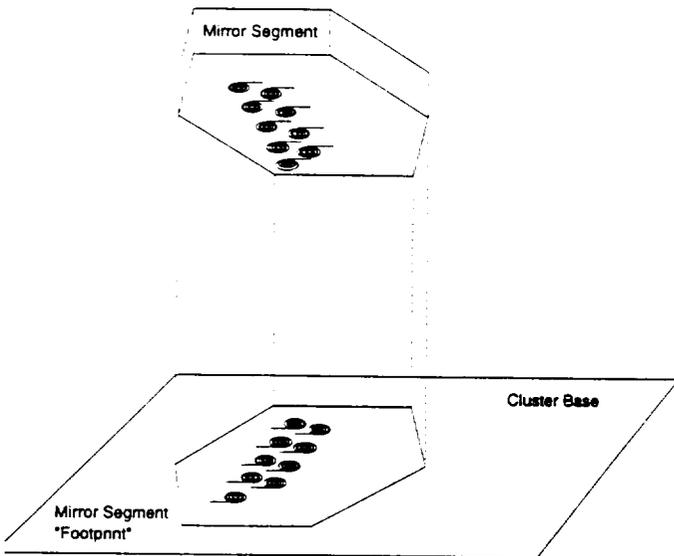
Figure 31: Illustrations of four of the segment attachment schemes considered.



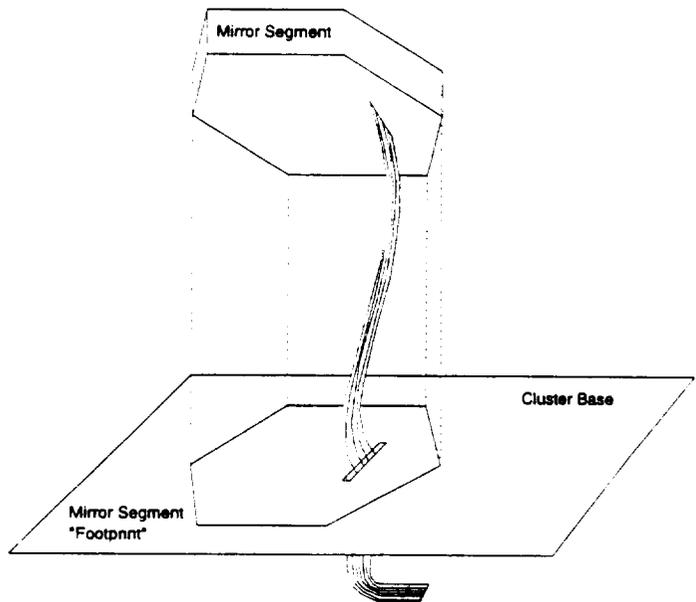
Finger & Pad Connection



Elastomer Conductor Connection



Inductive Coupling



Flexible Pigtail Connection

Figure 32: Illustrations of four possible methods of making electrical interconnection with the mirror assembly.

23.05cm

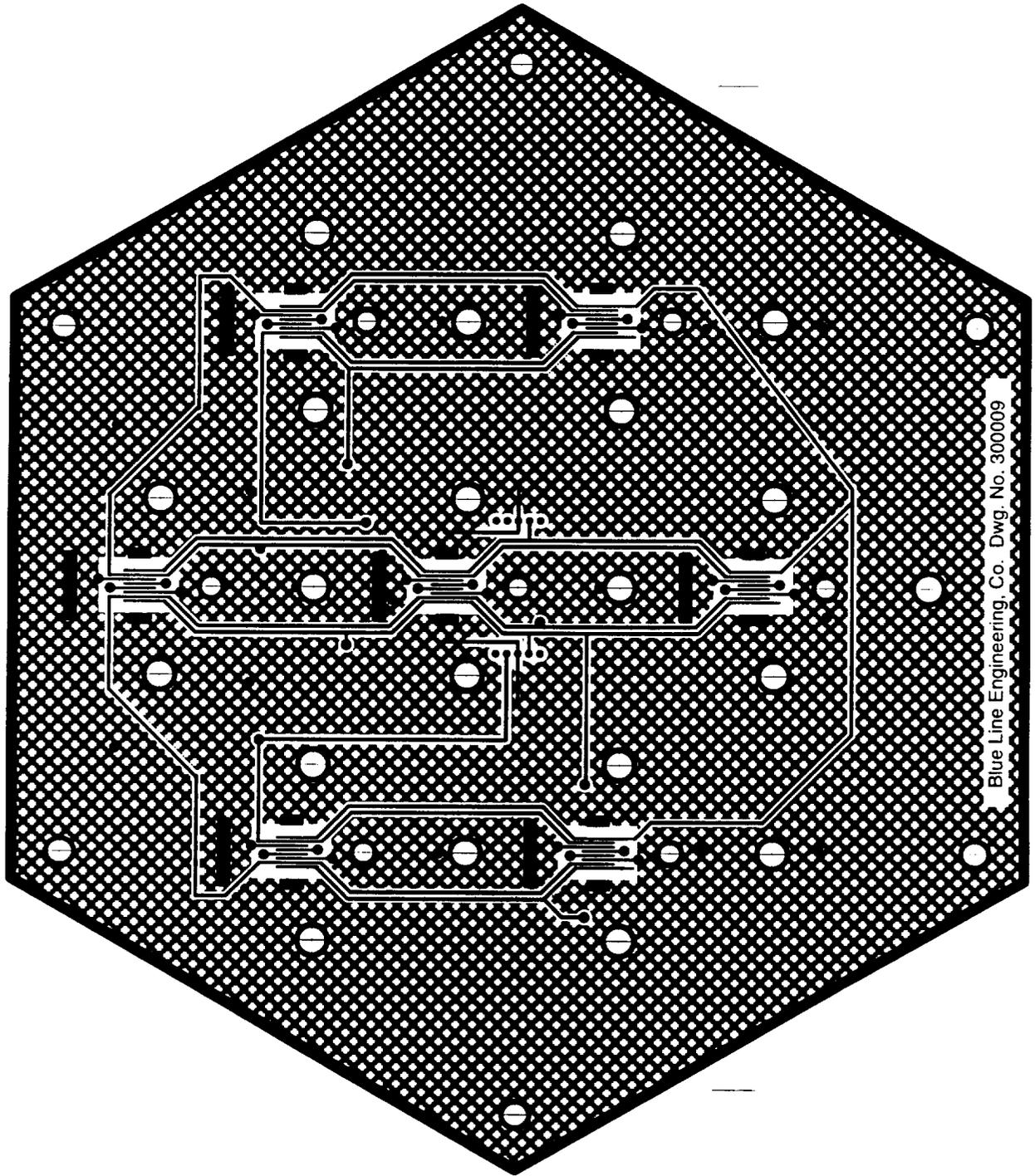


Figure 33: Layout drawing of cluster base back plate. Note that the layout provided for three equally spaced holes around a smaller central hole for each segment. These holes were used to provide access to the adjustment screws for attachment of each segment assembly. The small black rectangles are the locations where the slots were to be cut to permit passage of the flat flexible cable to pass through to make contact between segment and cluster base.

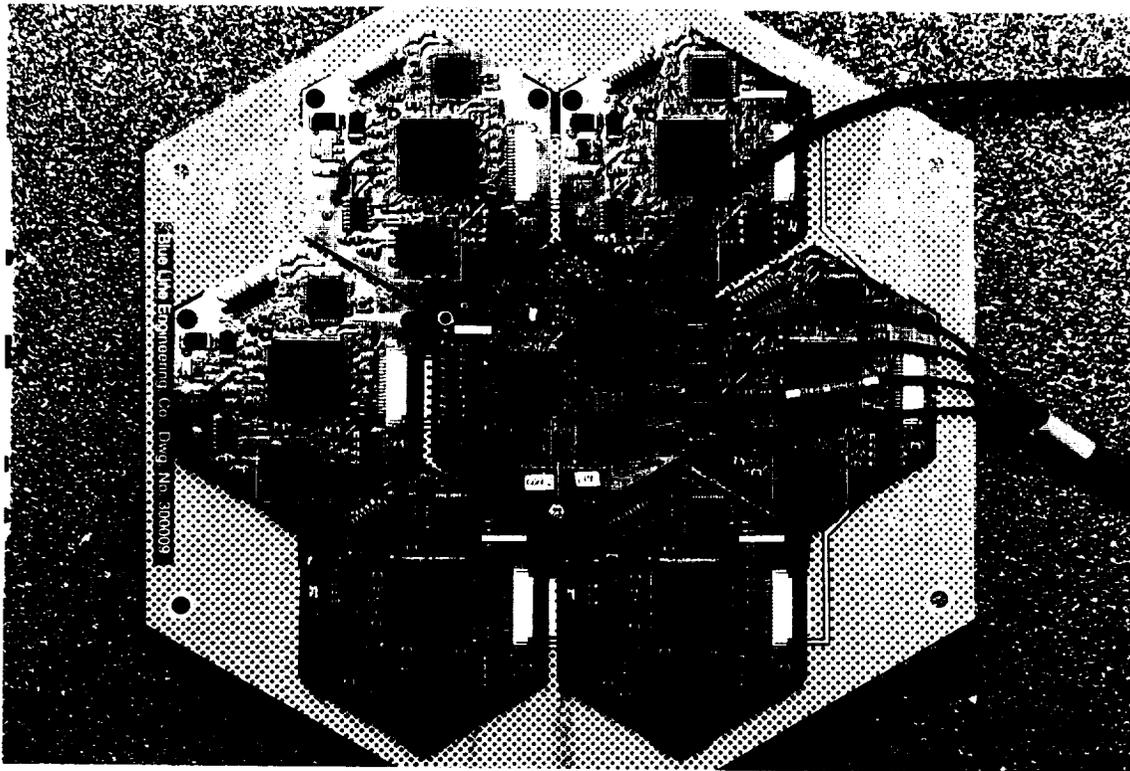


Figure 34: Photo of the first cluster base we constructed showing the installation of the segment processor boards and the Cluster Data Router/Concentrator (CDRC) which sits just above the processor board for the central segment.

Problems Encountered

The main problem we encountered was due to a decision at Blue Line late in the project to switch the SSD from an array of flat mirrors to an array with a 1 meter ROC. This problem was compounded by the decision to make a new cluster base using graphite-epoxy with Nomex honeycomb core. The concept of bonding aluminum cups into holes bored into the honeycomb structure was workable but required greater precision in machining tolerance than we were able to achieve in our laboratory.

During assembly of the SSD it became clear that the use of three screws with Belleville washers to achieve the required precision in all 6DOF was not working out as planned. A big part of the problem may be attributed to the lack of uniformity or precision in the segment assemblies. Still an even deeper part of the problem can be attributed to the confusion stemming from mixed objectives and priorities. Rather than simply demonstrating a new and important concept, we found ourselves also trying to meet the somewhat artificial (or at least premature) goals of mass, bulk, and elegance required for a highly portable briefcase demonstrator as pictured earlier in this report (see Figure 5).

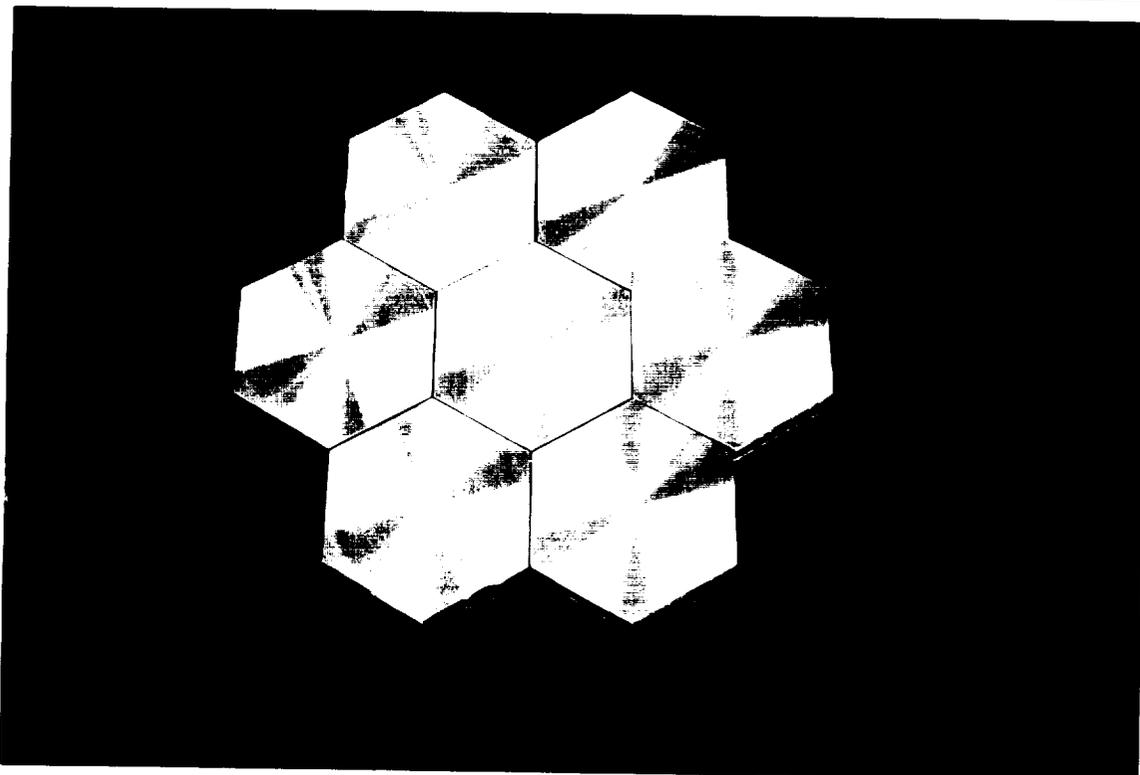
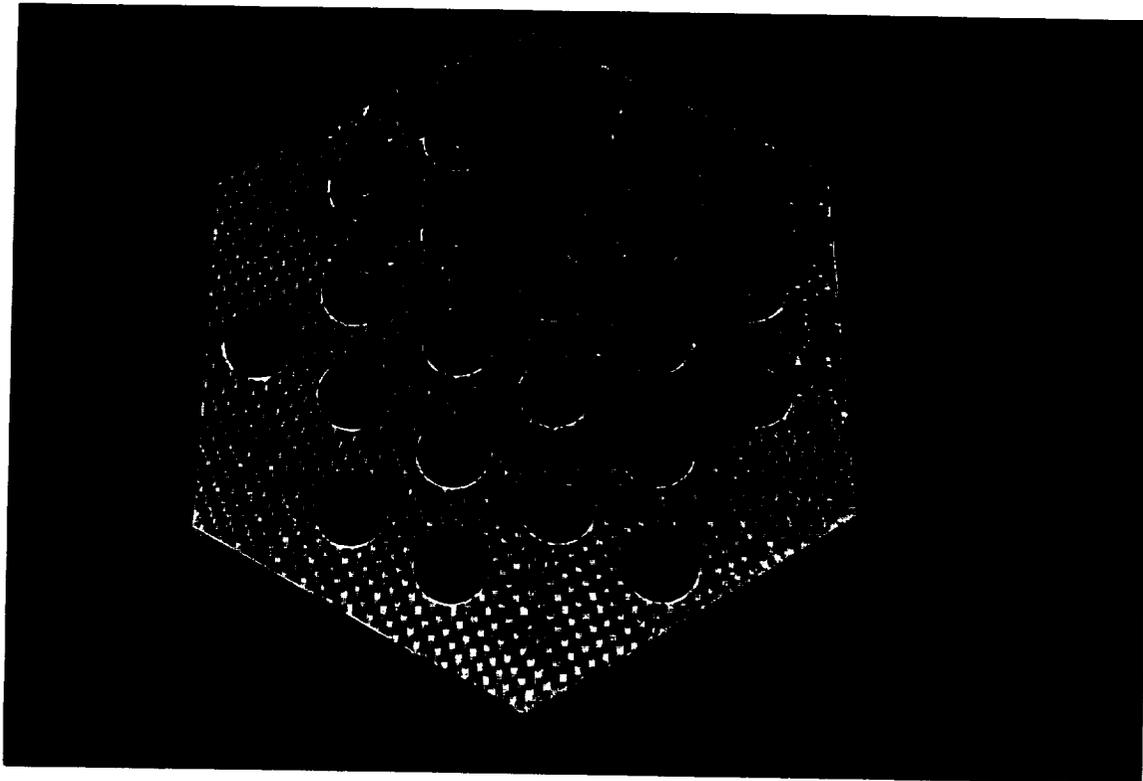


Figure 35: Photos of the Graphite-Epoxy version of the Cluster Base that we built for this project. The upper photo shows the aluminum cups that were recessed into the base at varying angles relative to the plane of the structure and bonded in place. The lower photo shows where the segments will be mounted. See Fig. 5 also.

Lessons Learned

Had we stayed with a flat segment array we would have had much greater success with the SSD prototype than we did. In retrospect we should have completely redesigned the cluster base when this change was made rather than try to modify the original design. As a conceptual prototype the cluster base achieved all of its goals. It does incorporate a printed circuit assembly as a main structural element and it does incorporate segment attachment provisions while serving as the only mechanical structure for support of the SSD mirror array. But the concept as it stands now is not readily extensible to either larger clusters (>0.5 m) or much smaller segments (≤ 5 cm).

Conclusions and Recommendations

Based on the results of our investigations, we have concluded that it is unlikely that integration of electronic distribution circuits into a composite structure would prove economically viable or even possible for clusters larger than about 0.5 m square. The problem is further compounded if the circuit must have a curved shape. In cases where the segments are larger than about 200 mm it probably makes more sense to produce a flex circuit that can be linked together in a variety of configurations to produce a large 2D circuit. For large arrays of small segments it is probably best to jumper together a few large circuit boards designed to butt up against each other. For smaller arrays the approach used for this research would work very well.

The greater issue that still needs further development is the issue of mounting segment assemblies onto the cluster base. The problem is especially difficult when the array must form a spherical or parabolic mirror. The best approach at this time is to construct the cluster support structure such that it has a faceted front surface where the slope of each facet is normal to the optical axis of a segment mounted to that facet. This would at least give the attachment mechanism for each segment a standard frame of reference.

The greater question that needs to be addressed is whether one would be better off to build the adjustment capability into the mirror segment itself and thereby dramatically simplify the attachment requirements. In this case the segment would have some sort of set-and-forget type long throw actuator that could position the mirror in tip/tilt and piston over a wide range, much greater than that allowed by the current ± 150 μm throw of the actuators. A very significant side benefit of such an approach would be that it would reduce the stroke requirement on the actuator itself to something on the order of ± 15 μm , which opens up a whole host of possibilities.

The alternative would be to shift more of the burden onto the attachment/alignment hardware such that one could manually align all of the mirrors to within say, ± 50 μm or better. Again this would allow one to relax the actuator stroke requirements. The point is that the current scheme requires the actuators to have much more stroke than is needed to correct for dynamic disturbances, whether they result from structural or atmospheric disturbances. Yet we have seen that it is still difficult to devise a low mass, low cost, workable solution that gets the mirror surfaces well within the correction range of the segment's actuators.

Our recommendation is to shift the burden onto the segment and to implement the equivalent of a small motorized mirror mount at the base of each segment. Segment attachment then becomes a bolt-in-place process and all one need worry about is ensuring that the gaps are within spec.

Task 3 — Mirror Technology Development

Per our understanding of the original intent of the SOW, Blue Line was to define the general requirements for the mirrors and work with project members at the US Naval Air Weapons Center at China Lake who were funded to do the actual fabrication and polishing of mirror segments. These segments were then to be delivered to Blue Line for test and further integration into the SSD project, and then delivered to NASA. Unfortunately this is not the way things worked out. As a consequence Blue Line was still on the hook to deliver segments in order to complete our Phase II SBIR, which was directed at the development of active segment assemblies.

The bottom line is that this turned out to be much more of an exploratory development effort than we had originally anticipated but in the end we did achieve our goals. In the discussions under this task we will provide a summary review of the many different efforts carried out to reach this goal. We should also note that significant portions of this effort were funded through our Phase II SBIR project, which also depended on successful development of mirror segments.

Technical Discussion

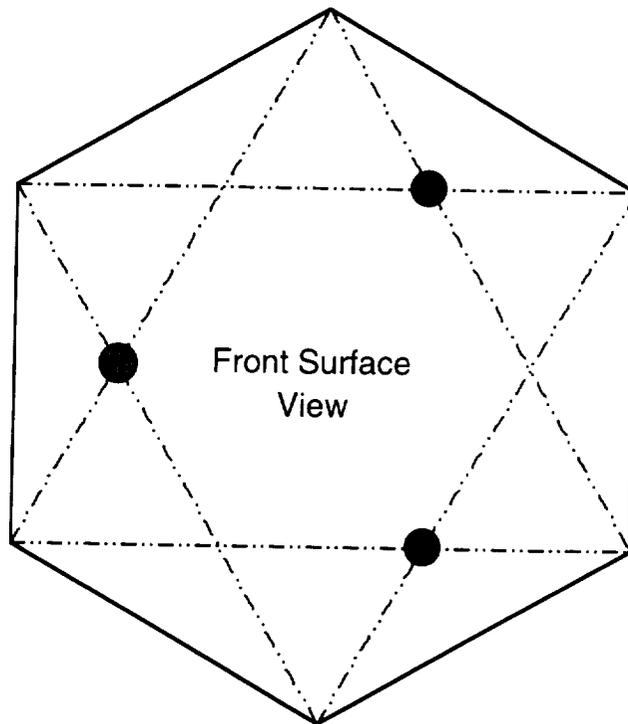
Defined requirements

The starting point for this task was to define the requirements for the mirror faceplate. These mirrors were intended to be used with the SSD. The SSD was to use an array of 7 flat hexagonal segments measuring 7 cm flat-to-flat. The main concern at the outset was to achieve the lowest mass possible with a production process that could lead to a low cost part. The baseline requirements for the mirrors are shown below:

Requirements for mirror segments:

Shape:	hexagonal
Dimensions:	(see sketch)
flat-to-flat	7 cm \pm 15 μ m
thickness	\leq 8 mm
Material:	TBD, Single Crystal Silicon preferred
Mass:	\leq 11 grams (goal)
	\leq 25.6 grams (worst case)
1st resonant frequency:	\geq 5 kHz
Mirror surface:	
radius of curvature:	∞ (flat surface)
accuracy:	$\leq \lambda/20$ RMS
reflectivity:	\geq 98% 0.4 μ m to 10.0 μ m
scratch & dig:	40-20 \AA
Edge sensor provisions:	TBD (assume no edge sensors for now)
Actuator attachment:	3 point per sketch
Attachment method:	TBD (compliant bonding likely)

● Relative location of actuator/flexure attachment points on back surface.



Laminated Silicon Mirrors

At the Preliminary Design Review held in May of 1996 at MSFC it became clear that the SSD project team could not identify any promising solutions that would meet the mirror requirements and objectives as we saw them at that time. One possible candidate solution was proposed by Blue Line. The suggestion was to try a concept first described by Greg Ames in 1993, which was to form the mirror by laminating chemically etched cross-sections of a ribbed mirror using standard double side polished single crystal silicon (SCS) wafers. The suggested approach was agreed upon and Blue Line began an effort to create the first mirrors of this type ever produced. At the same time Georgia Tech Research Institute embarked upon a parallel effort to produce mirror faceplates using electro-discharge machining (EDM) techniques to create a lightweight substrate using 3 mm thick SCS wafers.

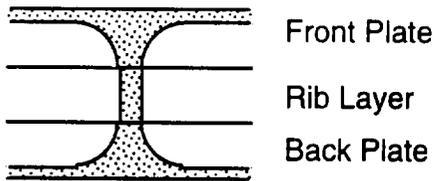
Blue Line's concept for laminated silicon mirrors grew out of work by the PI in the emerging technology area known as microelectromechanical systems (MEMS). In addition to leading to a novel means of constructing lightweighted mirror substrates using SCS, the concept also has the potential to include embedded sensors and/or actuators, and many other such features afforded by this industry. The idea is to build up the mirror substrate to the required thickness needed to give the final part the mechanical stiffness it needed. Since the standard wafer thickness for 100 mm wafers is about 500 μm , this meant that one would need to laminate a number of wafers together to achieve a final structure that was on the order of a few millimeters thick. We

estimated that the substrate would need to be 3 mm thick which would require 6 wafers of standard thickness.

In order to maximize the stiffness to mass ratio we would need to create a ribbed structure. We designed a dual level rib structure that featured both full depth ribs and 1 mm deep mini-ribs, sometimes referred to as cathedral arch ribs. The mini-ribs help to reduce plate deflections between the full depth ribs during mechanical polishing processes. To verify the design concept we contracted ROM Engineering of Tucson, AZ to perform finite element analyses. The results of that study indicated that the proposed structure would meet the mechanical design requirements. Relevant data on proposed design is listed below:

face sheet thickness	500 μm
back plate thickness	500 μm
rib dimensions	1 mm wide 1.9 mm high
overall thickness	2.5 mm
rib pattern	similar to main rib structure in Phase II PAMELA
density of SCS	2.328 grams/cm ³
Young's modulus	1.9x10 ¹² dyne/cm ² (close to stainless steel)
Knoop hardness	850
tensile yield strength	6.9x10 ¹⁰ dyne/cm ²

The basic concept is illustrated in Figures 36 & 37. Note that for 7 cm segments we can only obtain one segment from a stack of 6 standard 100 mm silicon wafers. Whereas for 2.8 cm segments one can obtain 7 segments from the same size wafers and it only requires a stack of 3 wafers to meet mechanical stiffness requirements.



Cross-section detail of rib structure.

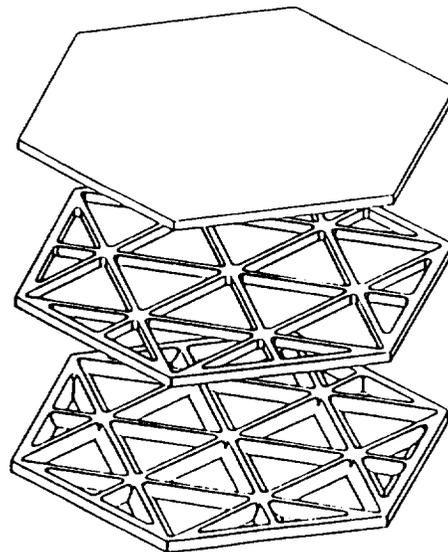


Figure 36: Exploded diagram of a single mirror showing lightweighted front plate, middle rib structure, and lightweighted back plate. Note that significant material has been removed from both front and back plate but a continuous exterior surface is left intact and rib structure is etched completely through.

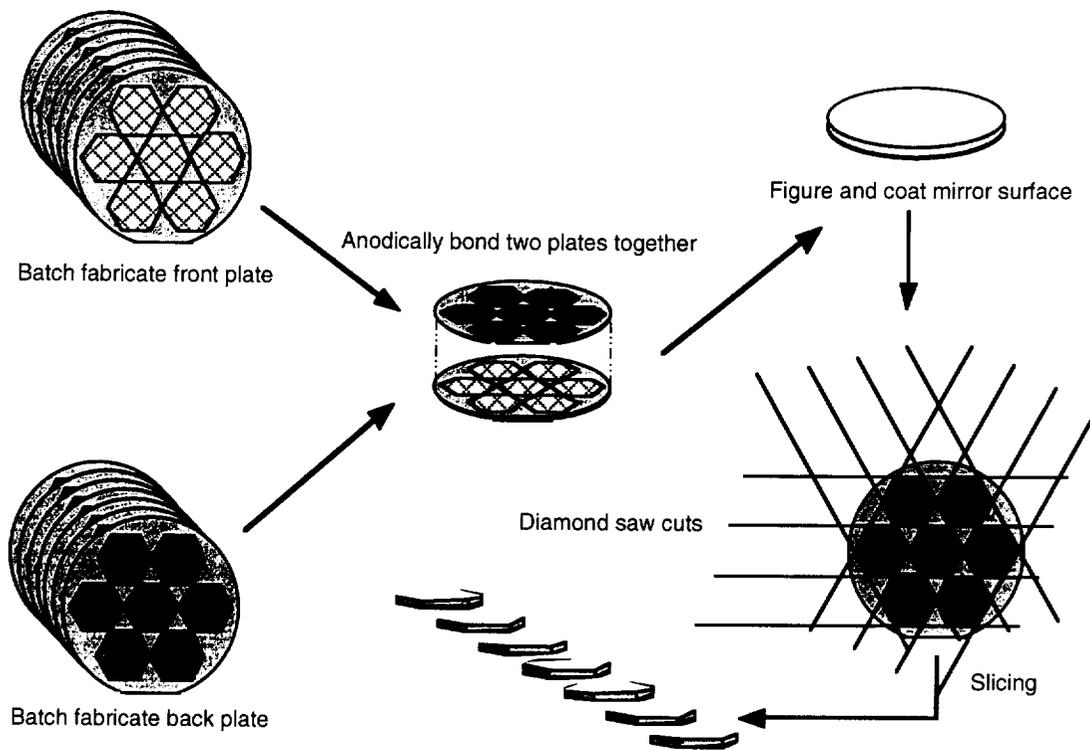


Figure 37: Illustrations of general concept for mass production of laminated silicon mirrors. This illustration depicts a process that yields 7 small mirror segments from standard 100 mm wafers.

The experimental work was carried out at the Microelectronics Research Laboratory (MRL) at the University of Colorado at Colorado Springs. The PI for this project, Greg Ames, is very familiar with semiconductor processes and conducted most of the cleanroom work.

The process required the use of etching solutions that could quickly etch through about 250 μm , which is about half the thickness of a standard 100 mm silicon wafer. The etchant we used is known as HNA. It is an isotropic etchant composed of hydrofluoric acid, nitric acid, and acetic acid. Etch rate is dependant on the relative mixture and temperature of the acid bath. In order to preserve the life of the acid bath and reduce the amount of toxic gasses produced we chose to etch channels around the piece to be removed rather than simply etching away the entire area. This is what we mean by cutting out the areas between ribs.

The first step was to develop a double sided photolithography process. Since the mask aligner at the UCCS laboratory did not have this capability we had to create our own. Fortunately we did not require a great deal of precision in aligning the two masks. Good visual alignment would suffice. Also, since we were not dealing with semiconductor scale devices, we could utilize inexpensive film type masks. The device we came up with is a pin registered mask frame which sandwiches the wafer between the two masks. It fits under a standard mask aligner and one simply exposes one side, flips the device over and exposes the other.

The next step was to draw up the masks. This was done on a Macintosh computer. Four mask sets were drawn up, and each set consisted of a front and back mask. The four layers were facesheet, mini rib layer, main rib layer, and back plate. The rib layers and back plate were designed to provide recesses in the edges of the segment once the final hex was cut from the

laminated stack. The facesheet did not have these recesses so it would overhang the edge sensors. The back plate included vent holes so that there were no closed chambers to entrap air or chemicals in the finished substrate. The four different mask layers are shown in Figure 38.

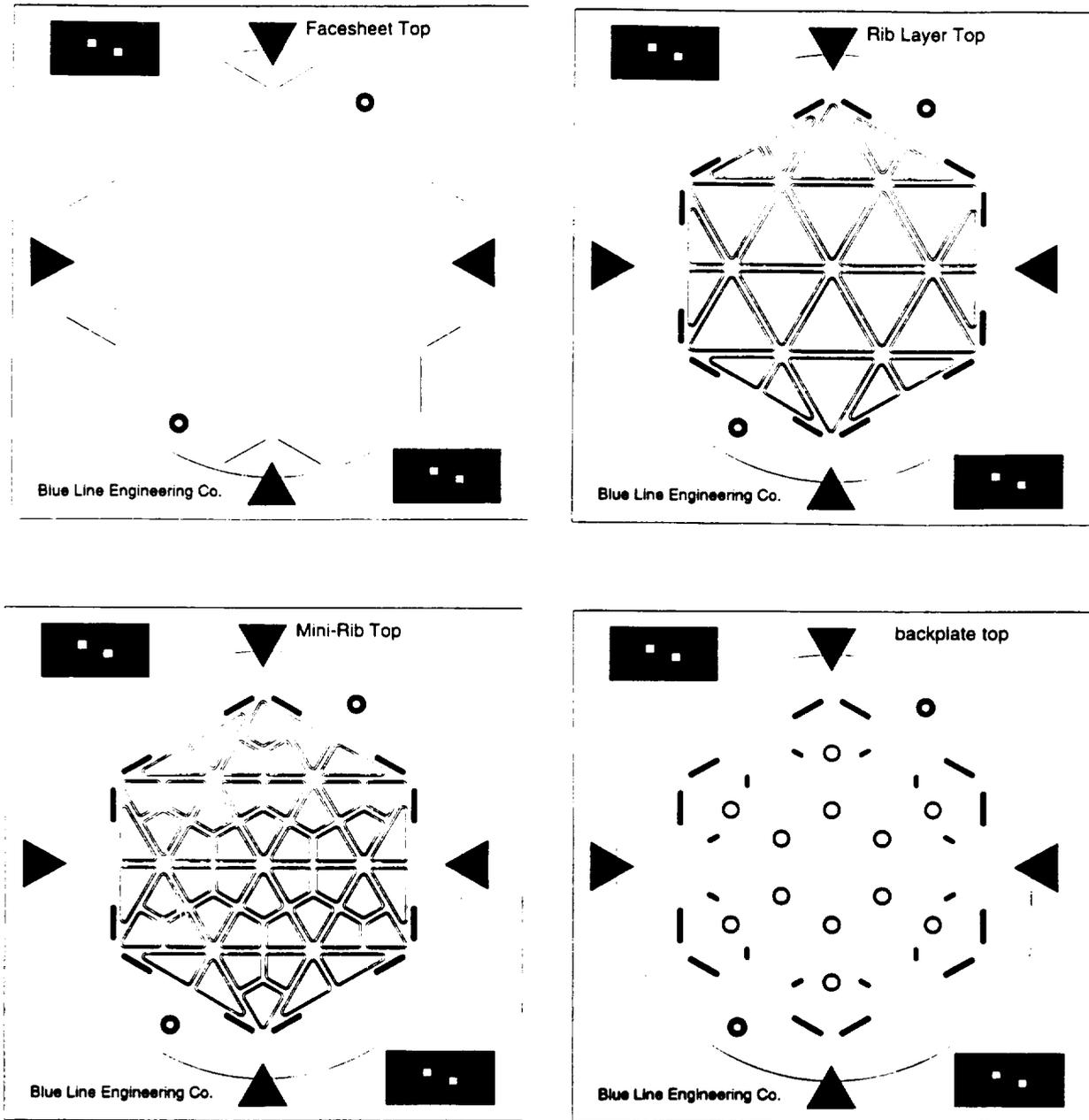


Figure 38: Four different mask layers used in laminated silicon mirror work. We note that each finished substrate would require one facesheet, one mini-rib layer, four rib layers, and one back plate for a total of seven wafers.

The photolithography processes went very well. The etching process took some effort to devise methods to prevent thermal runaway, but we did achieve very good results with well defined rib layers. At first we had problems with pits on the front surface due to pinholes in the silicon nitride mask, but we simply applied a thin layer of wax on that surface to solve the problem.

The silicon nitride mask was stripped in a reaction ion etching chamber with good results. All in all we had very good success in producing the individual silicon layers with very little breakage or loss, other than early experimental efforts. But the process was quite time consuming and resulted in the PI for this and other projects being tied up in the lab for much of the time.

The final step was to anodically bond the stack of wafers together. We had successfully demonstrated the ability to bond two clean wafers together very early in the effort. In fact, this was the first thing we did to establish the feasibility of the concept. Several wafers were bonded together with excellent results. As far as we could determine we had perfect bonding over 100% of the mating surfaces. The process went so easily and so well that we did not expect the difficulties we encountered when attempting to bond the etched layers.

We tried a number of different remedies and techniques. We even attempted to use adhesives, all without success. Finally it became clear that this technique of fabricating mirrors was turning into a major research effort in itself and we still had not begun to address the issues of figuring the front surface.

By this time we had also concluded that the approach was limited to very slow or flat mirrors since the creation of mirrors with more than 500 μm of sag would result in extremely thin facesheets at the center of the segment. It was also becoming clear to Blue Line personnel that while in theory one could take advantage of batch processes, the reality was that it was still going to be an expensive approach to substrate fabrication for the foreseeable future. The conclusion was that we should abandon this effort and seek a workable, though perhaps less remarkable, means of providing mirrors for the SSD.

Flats vs. Spherical Surfaces

Once it became clear that we needed to look for other approaches to producing mirrors, we also decided to take a fresh look at the question of flat vs. spherical front surfaces. Flat mirrors are easier to make in some respects since one does not need to worry about radius of curvature matching. Flats are also easy to work with in a laboratory setting where one can use large beam expanders and interferometers to measure performance.

But in a stand-alone demonstrator designed to be showcased in a conference room setting, a spherical surface has several advantages. First, one can implement several demonstrations based on center of curvature measurements (see Figure 39). These can provide meaningful demonstrations and measurements of the active control of segmented arrays. With flats one would be limited to visual observation of the mirror only since large beam expanders would be too bulky and expensive for the sort of briefcase demo we had in mind for the SSD.

Another reason for switching to spherical mirror figures was that in the long run the potential applications for segmented primary mirror arrays would require curved, not flat, front surfaces. While the decision to switch from flat to curved front surfaces for this stage of development would prove to cause many complications throughout the system, the change at least had the benefit of pointing out those interdependencies.

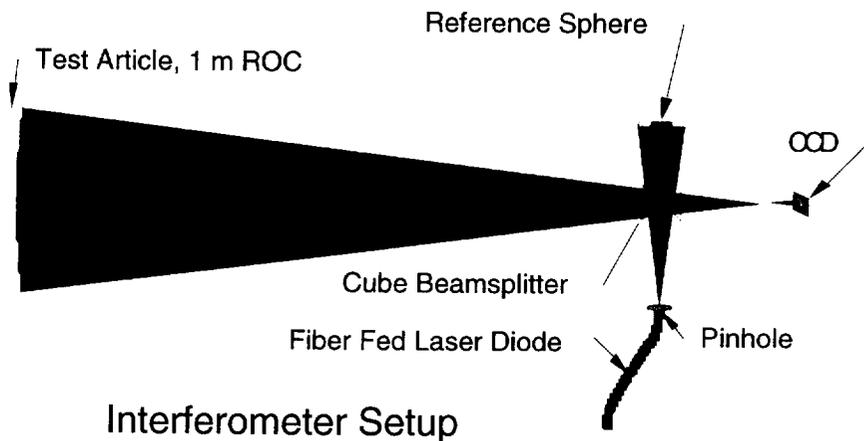
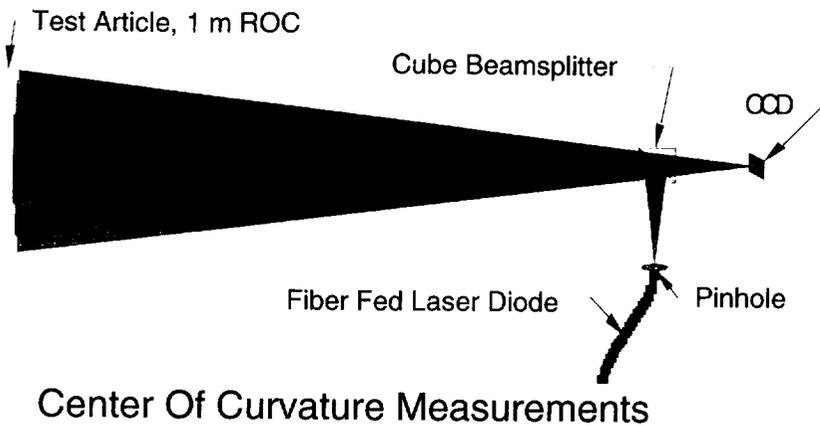


Figure 39: Two possible test arrangements that reference the center of curvature.

Glass, SiC, Al

We considered other substrate materials in addition to single crystal silicon: glass, silicon carbide (SiC), 6061 aluminum, and Vanasil. We learned something interesting from each of these explorations, as will be discussed in following paragraphs.

As early as the summer of 1996 we began looking into simple low cost glass solutions as part of a “midnight oil” type project. The goal was to see if we could grind our own mirrors using the same tools and techniques that amateur telescope makers worldwide have employed for many past generations with great success (see Figure 40). While we recognized that this approach was not really suitable for NASA or DoD type missions, we felt that a simpler and much less costly solution was needed if this technology was ever going to succeed as a product for the amateur astronomy markets.

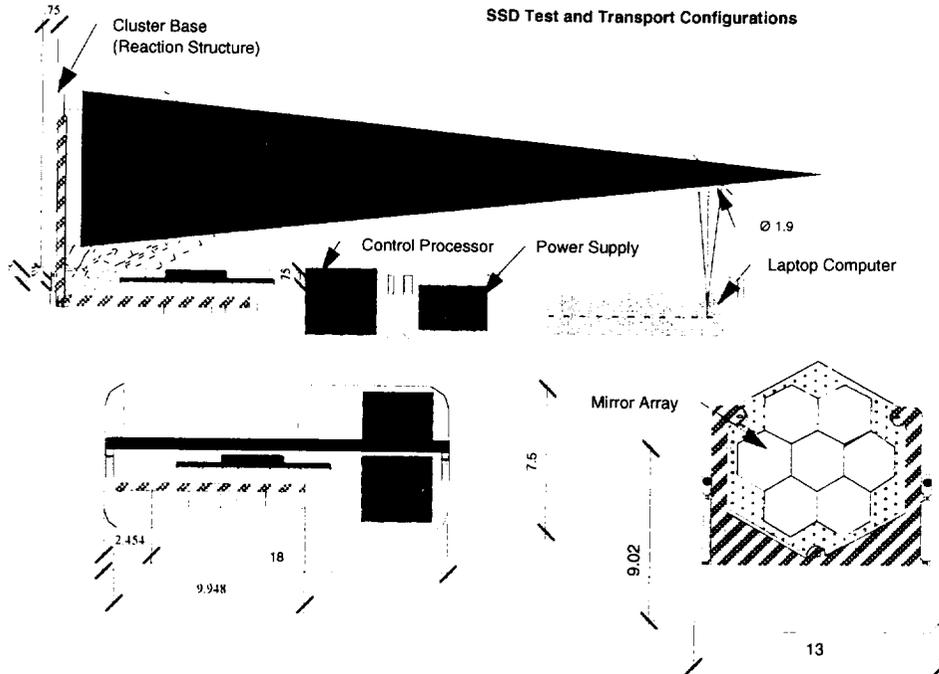


Figure 39A: This drawing illustrates why we chose a spherical array for the SSD.

The question of why—or why not—use glass often comes up. There are many grades of glass that can be considered for substrate materials: ULE, Zerodur, and Pyrex, to name a few. All are relatively easy to grind and polish. Glass is a stable substrate material — it does not creep with age or exposure to thermal cycles. And there are many potential vendors or manufacturers to choose from. But glass is difficult to lightweight, as we learned in the PAMELA telescope. Also, it is difficult to include physical or mechanical features for such things as edge sensor installation or actuator attachment.

Still, if one can live with the higher mass and if one does not need edge sensors, glass may be the answer. As mentioned earlier, we attempted to hand grind our own mirrors as part of an unfunded IR&D effort. We did not succeed. Grinding went very well but the final polishing stages always ended up with all kinds of print-through due to the attachment of the hexes to the workpiece. Someday, when we get the motivation to give it another try, we will look more carefully at methods of blocking the mirror segments along the lines of methods employed the University of Arizona’s Stewart Lab.

We also received both flat and spherical hexagonal mirror “samples” from Zygo. One of these can be seen in Figure 41. These were great mirrors but the purchase price for even production quantities was in the \$600 range and when we imposed tighter radius of curvature (ROC) requirements, the price shot up above \$1,000 each. This pretty well defeats the cost advantage of glass, so we started looking for other solutions.

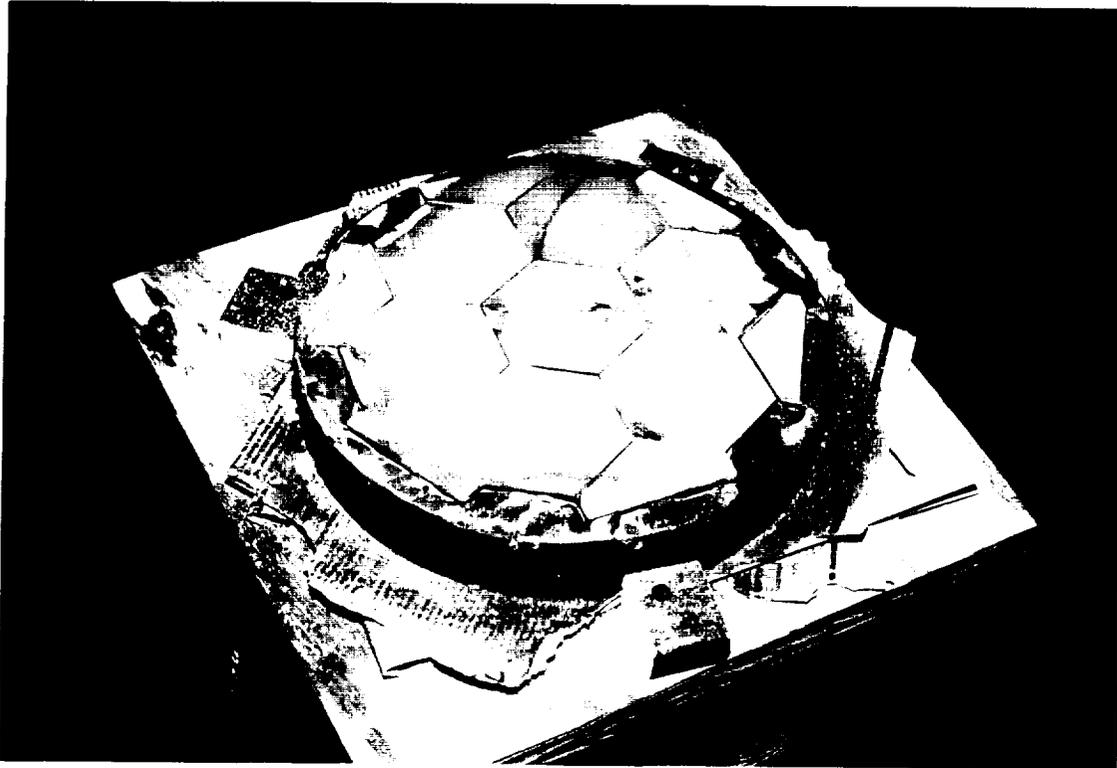


Figure 40: Blue Line's after hours attempts to hand grind and polish an array of 7 segments.

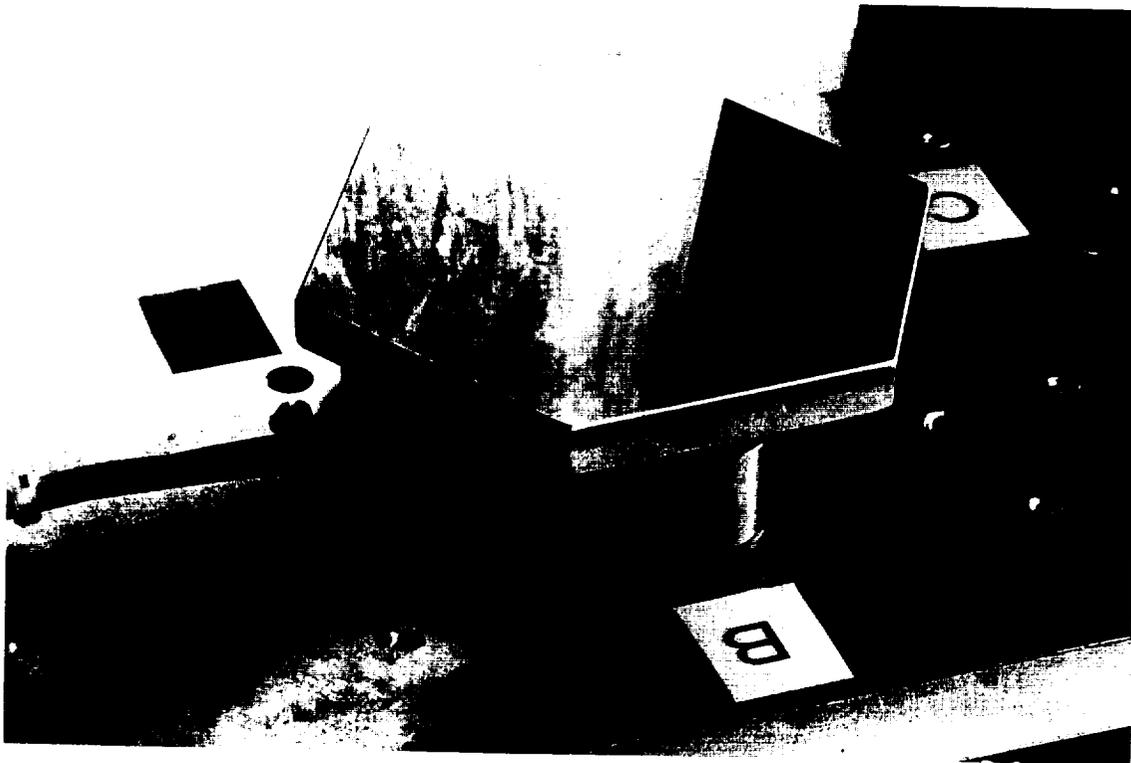


Figure 41: This flat 7 cm glass mirror was provided as an evaluation sample by Zygo Corporation.

One of the first materials we shopped around for was SiC. We learned two interesting things along the way. First, the commercial landscape in SiC mirror production has undergone a great deal of change since the start of this decade. Most of the original companies have either gotten out of the business or sold off their technology to new ventures. Still we did get cost estimates for SiC substrates and as expected they were prohibitively expensive for our needs.

At this point the discussion will jump to the issue of ROC matching, which ultimately led us to the solution we finally settled on. We will then continue the discussion of the aluminum substrate materials we considered.

ROC Matching

One of the lessons that keeps getting driven home through this research was the need for tight ROC matching between segments — and how difficult it is to achieve. We have developed computer programs to estimate the phase error due to ROC mismatches as a function of segment size, position in the array, type of figure (spherical or parabolic), speed of primary, ROC error, and in-plane errors (translation of segment along the optical surface). We found, for instance that one could approximate a parabola with spherical segments if the f# of the primary is on the order of f6 or greater.

But we also found that even slight ROC mismatches in a spherical primary with an f# on the order of f2 or less could be very demanding. For example, the SSD was to have a 7 segment spherical primary with a ROC of 1 meter. An error in the ROC of 160 μm would result in a phase error of roughly 32 nm, or $\lambda/20$. The difficulty of meeting these requirements are what led us to rule out commercial sources, many of whom would not even bid on the requirements. This is also why we attempted to grind and polish all seven segments as a single mirror. Even though we have not succeeded in this effort to-date, this is clearly the approach for small arrays.

The best solution for tight ROC matching is a technique known as optical replication. The method we will be discussing should not be confused with replicated optics techniques developed by MSFC, GSFC and others. The technique we will be discussing is one where an optical surface is deposited onto a glass master and the substrate is then bonded to the deposition. By means of thermal shock, the part is released from the master such that the optical surface is now transferred to the substrate. This was the approach we followed to solve the ROC issue.

Replicated Front Surfaces

One means of assuring that ROC tolerances are met is to employ a technique known as first surface replication. This technique had actually been used successfully by Kaman in Phase I of the PAMELA project. The process is capable of producing nearly identical mirror surfaces, including flats, spheres, and parabolas. For some reason the technique has never really gained wide acceptance though it does produce good results.

The process involves producing a production master, which is the complement or negative of the optical surface to be produced. This master must be figured and polished to the same degree of accuracy and precision as the final part specifications. Once prepared, a metallization layer is deposited onto the master, an adhesive layer is applied, and the substrate is registered and pressed onto the master. Using thermal shock methods, the part is “popped” off the master with

the mirror surface intact, now bonded to the substrate. This process relaxes the tolerances on the front surface figure accuracy for the raw substrate quite a bit. It also makes it possible to economically finish substrate materials that would otherwise require expensive filling and figuring processes as is the case with SiC substrates.

Cast Vanasil

Vanasil is an age-hardenable hypereutectic aluminum-silicon casting alloy. It has a lower coefficient of thermal expansion than 6061 aluminum (15 ppm/°C vs. 22.5 ppm/°C) and typically higher modulus of elasticity (93—103 GPa vs. 68 GPa) at equal or slightly lower density ($\approx 2.7 \text{ g/cm}^3$). Also, Vanasil is reported to be more stable as a mirror substrate in cryogenic applications, but special heat treatment is required. The higher specific stiffness of Vanasil vs. 6061 Al, together with the promise of low cost casting processes in high volume production is what attracted us to this material.

After locating a firm in Canada that had experience in casting Vanasil, we drew up a ribbed structure and had SLA patterns made. One of these patterns appears in Figure 42. These patterns were intended to be used in a rapid prototyping process by the casting house. Unfortunately the pattern maker did not drain the parts properly with the result that the pattern had solid walls and ribs instead of having a honey-comb like interior structure which would allow the pattern to be burned out in the rapid prototyping process.

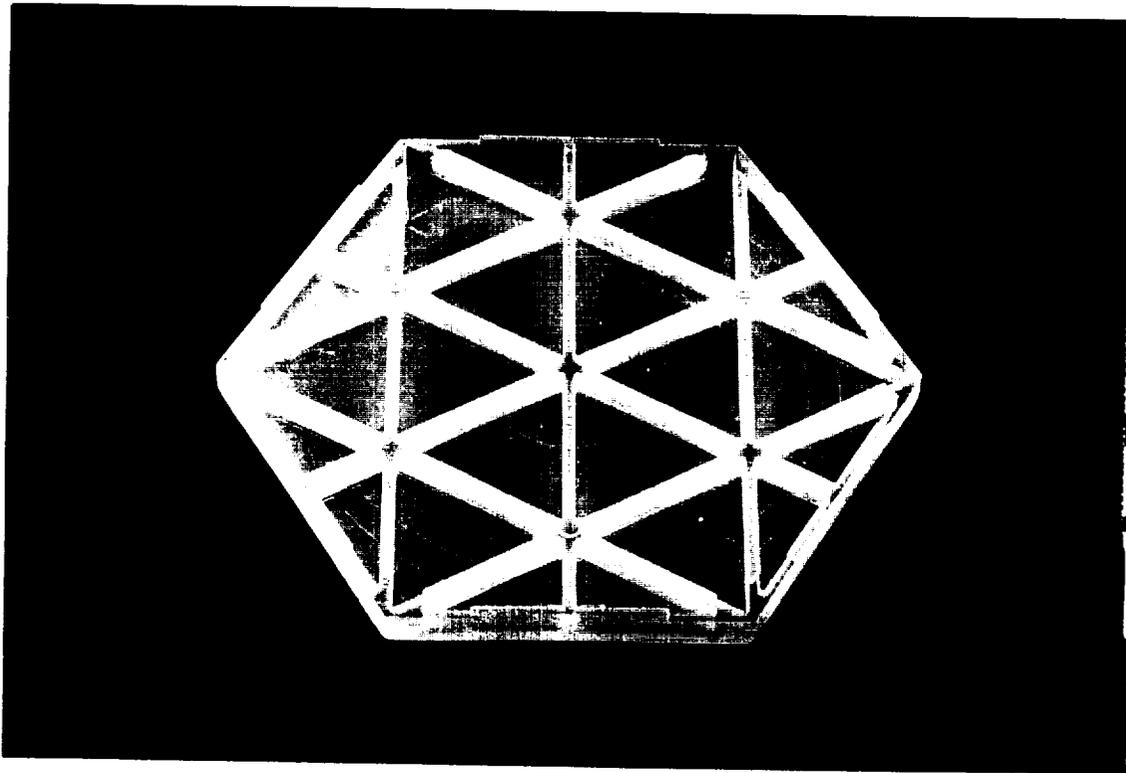


Figure 42: SLA pattern produced by stereo lithography for investment casting processes.

The result was that the casting house would not risk using the patterns as delivered. Since this turn of events took place fairly late in the project, we abandoned this line of approach in favor of machined aluminum substrates—as will be discussed in the next section.

Heat Treated 6061 Al

As interesting as rapid prototyping of cast aluminum substrates may be, it is difficult to justify the time and expense for a development project. The most direct approach is to just machine the aluminum substrates. Researchers had reported good results with 6061 aluminum when proper heat treatment schedules are used.

The final solution for the mirrors turned out to be machined aluminum mirrors. We show the back sides of an array of seven mirror substrates in Figure 43. These substrates were then delivered to the firm we selected to create the replicated front surfaces.

Provisions for Edge Sensors

Inspection of Figures 42 and 43 reveals that we included small recessed areas at the six corners of the substrate. These were the locations where the edge sensors were to be mounted. Given the difficulties that GTRI ran into in mounting sensors on the edges of the segments (see Figure 44 for illustration of original concept) and the unsuccessful effort to get SY Technology’s integrated circuit type edge sensors to work, we opted to use conventionally wound coils in machined ceramic housings (see Figure 45).

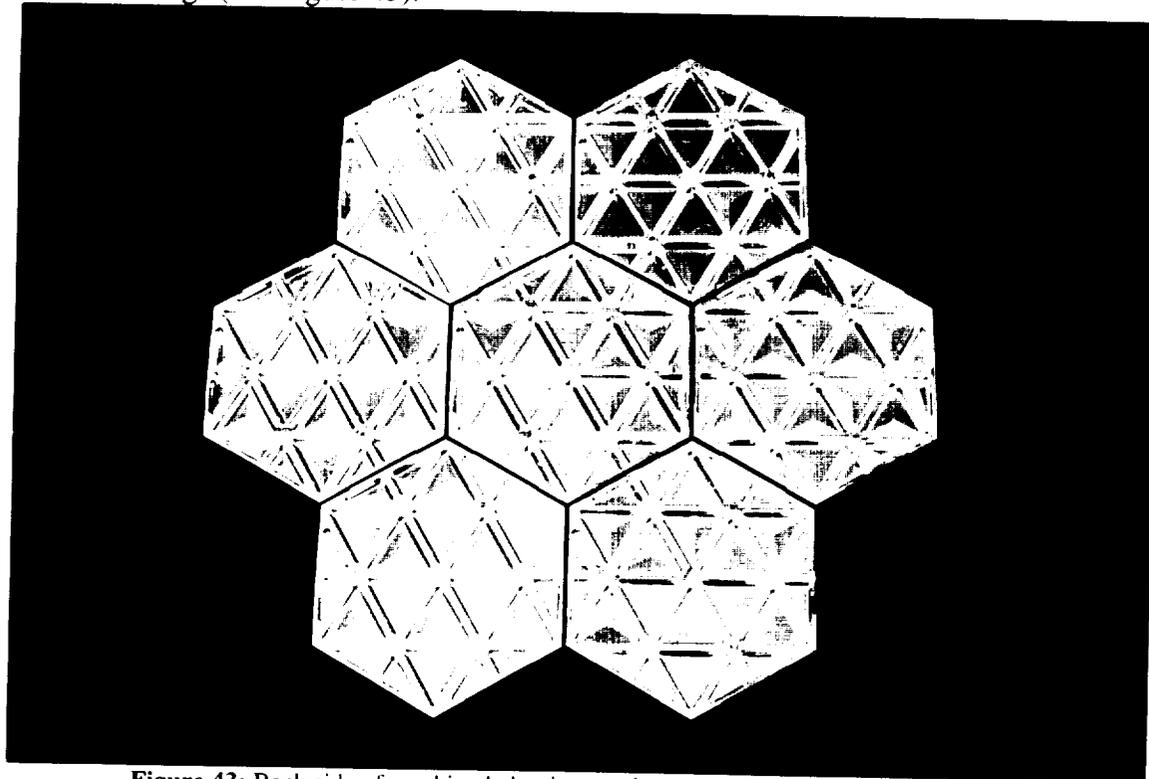


Figure 43: Back side of machined aluminum substrates that were eventually used on SSD.

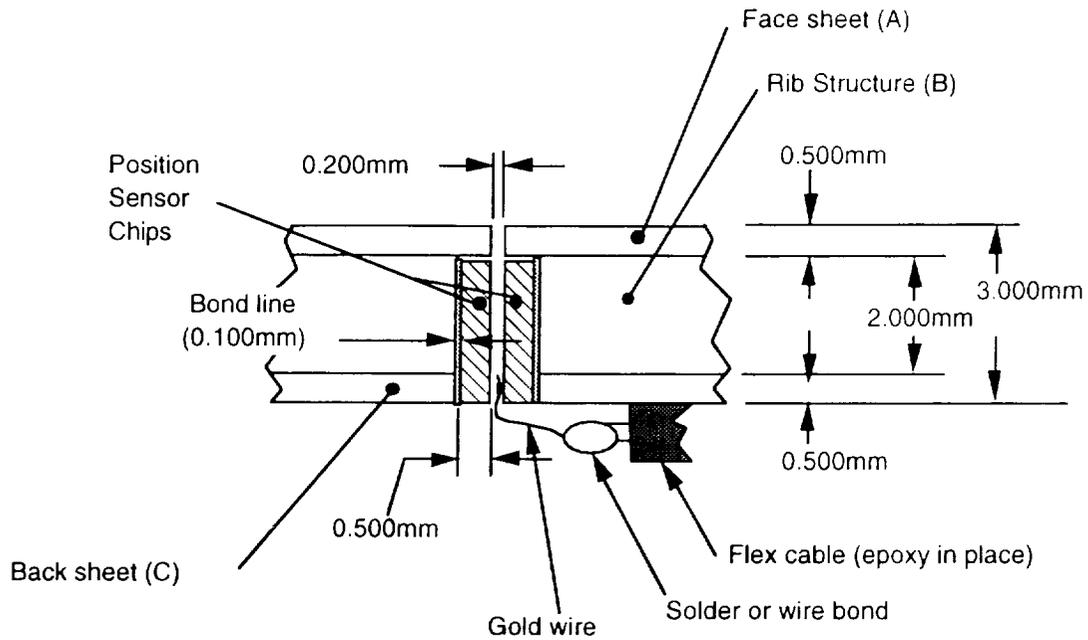


Figure 44: Early efforts were directed at segment designs that provided recesses or pockets in the edges of the segments to accept integrated circuit type position sensors.

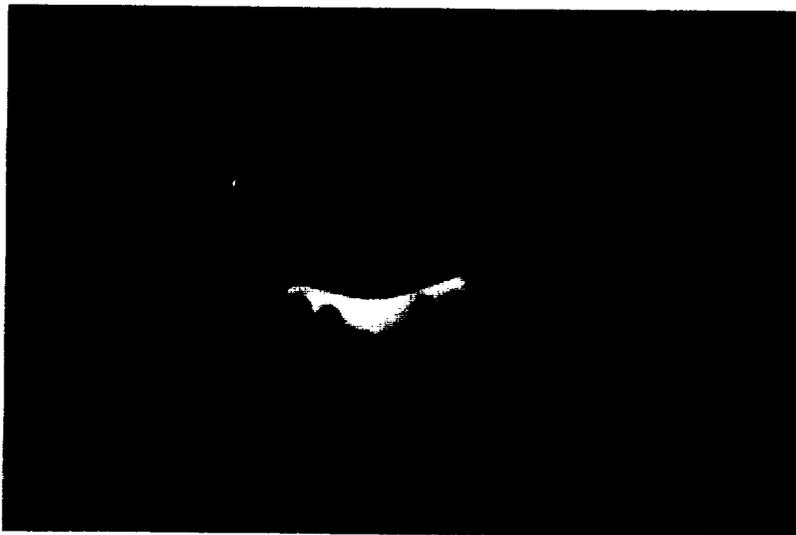


Figure 45: Inductive edge sensor housing that was to be bonded to the back side of the mirror. Each coil measures roughly 1.5 mm in diameter.

The chevron shaped coil housings shown in Figure 44 were to be glued to the back side of the mirror substrate in the corner locations, as noted earlier. In order to increase the amount of clearance behind the segment, we decided to add the recesses. This also had the effect of moving

the measurement point closer to the front surface of the mirror, which is good. More information on the integration of mirror segments is provided in the Phase II final report.

Actuator Attachment

Previous mirror designs for the PAMELA telescope had always provided blind holes in the back side of the substrate for actuator attachment. Typically a flexure or threaded insert is bonded into the hole as an attachment point to the mirror. This often resulted in slight dimples or bumps in the surface. While the effect on the overall figure error was negligible, it always provoked comment and concern from those examining interferograms.

For the machined aluminum mirrors we chose to provide small studs on the back surface at the intersection of 6 ribs. These studs are just barely discernable in the photograph of Figure 43. A top-hat like attachment was then placed over the stud and bonded in place. The flexure was in turn inserted into the top-hat attachment point and secured with a set screw. We did not detect any evidence of bumps or dimples in the interferograms.

Problems Encountered

Wafer-To-Wafer Bonding

As noted earlier in this report, we encountered problems with the wafer-to-wafer bonding of laminated segments. We were successful at initial demonstration tests where we bonded two unetched wafers together. The results were excellent and so easily accomplished, we did not anticipate the difficulties to come.

Two factors combined to make the lamination process much more difficult than the demonstration tests. First, it is necessary to laminate not just one pair but a whole stack of wafers together with nearly 100% bonding in the contact area. Second, the individual layers of the stack must be fairly well aligned with each other. This rules out any wringing or sliding motion.

We tried hydrating the wafer layers, elevated temperatures, vacuum bag loading, and adhesives, among other things. None were satisfactory. We do not think that it is impossible to accomplish this task. But most likely it would take quite a bit more experimental work, and most likely the creation of some special tooling, to achieve the sort of reliable and high quality bonding we need.

ROC Matching

In the course of this research we developed a deep appreciation for the importance of—and difficulty of—maintaining adequate ROC matching between mirror elements in a segmented array. We developed some analytic tools to help us quantify the required accuracy for future system designs. We also identified two candidate solutions: replicated optics, and grinding and polishing of all the mirrors in the array as one unit.

While replicated optics seems to offer a very cost effective solution for ground based ambient conditions, the epoxies are not likely to be suitable for long duration space-based applications. Also, as we found out in later work, the technique is best suited to relatively small mirror segments and may not be applicable for segments much larger than 33 cm.

As for grinding and polishing the segments as a single unit, this solution also has limitations. While it may work well for small arrays of small segments, it is likely to become increasingly problematic for arrays on the order of 1 meter or larger. Also, as with the wafer-to-wafer bonding, further experimental work is needed to arrive at a workable procedure.

Lightweighting

The need for low mass mirror segments causes difficulties in a number of ways. For one, it all but rules out certain materials, such as glass, for segments smaller than about 12 cm. It also drives up cost and design complexity. And finally, it dramatically reduces the number of firms that can supply the substrates unless a machined aluminum design is adopted.

Lessons Learned

The number of technical lessons we learned in this effort are too numerous to adequately represent here. Many different aspects of several different technologies were covered. But the biggest lesson we learned was that developing a low cost mass producible mirror that meets our requirements is a significant research and development effort by itself.

Machined Al with replicated front surfaces is a good solution for many terrestrial applications. It may be an ideal solution for commercial astronomical markets.

Laminated SCS may be a great solution for certain special applications or for segments no larger than about 3 cm but it is not likely to be cost effective for segments 7 cm and larger. Furthermore, laminated SCS not a good solution where the front surface has significant curvature.

Conclusions and Recommendations

In spite of the obvious difficulties encountered, this portion of the project should be viewed as highly successful in exploring a number of new techniques and materials for production of small lightweight mirrors. The methods of laminated silicon, cast Vanasil, and group grinding and polishing operations all warrant further investigation. But the key to success is to focus a single research and development effort on a single technique with well defined—and realistic—requirements and objectives.

Lastly, we see little market potential for active mirror segments on the scale of 7 cm as primary mirror elements. The only possible application for segmented mirror technology at this scale is use as a fast steering mirror for image stabilization.

SURPRISES AND OPPORTUNITIES

In recent years Blue Line Engineering Co. has been in close contact with project personnel at the McDonald Observatory's Hobby Eberly Telescope in regards to the recognized need for a figure maintenance system to keep the 91 segment primary mirror aligned. The modular processing system developed under this contract is ideally suited to the task and will serve as the baseline hardware/software architecture for any proposed figure maintenance system. With the prospect of this utilization of this technology comes the opportunity to further refine the state of the technology. Any such upgrades or improvements will be made available to NASA personnel at MSFC for use in the system installed on the PAMELA testbed if desired.

In a similar manner, Blue Line plans to use this processing architecture as the foundation for its new FAST telescope, to be developed over the next two years under NASA's SBIR program. Again, any substantive improvements or refinements to the basic system will be made available to NASA personnel. As a result of implementation of this system on these and other applications, one can expect to see numerous opportunities to make evolutionary advances in this technology.

MOTIVATION FOR CONTINUED RESEARCH

As noted earlier in this report, when the initial award of this contract was made the main interest in segmented mirror technology at NASA stemmed from initiatives to beam power to receivers in orbit about the earth, whether geosynchronous satellite or lunar surface. At that time segmented primary mirror systems seemed to offer the most viable approach to construction of large aperture ground-based beam directors capable of adaptive compensation for atmospheric turbulence effects. Since that time the interest in high energy beam directors has waned or at least gone dormant for some period of time. Currently there is a strong push toward a plethora of advanced astronomical instruments in space, most of which will require some sort of segmented primary mirror system to achieve their intended goals.

The fact that segmented primary mirror systems continue to emerge as one of the most critical aspects of next generation optical systems for such a disparate range of missions is in itself evidence that the sort of research conducted under this contract should be continued. Clearly segmented mirror systems will play a role in NASA's future missions for some time to come. Even as researchers try to peer beyond the horizon to large membrane type mirrors with areal mass densities below 1 kg/m², we predict that the need for a systematic approach to integrating large numbers of sensors and actuators will remain.

While the extensible and modular processing system developed and delivered under this contract represents a substantial improvement over prior technology, much work remains to be done to fully take advantage of this technology. The main area where further research and development is needed is in the form of software development utilities that will allow engineers to seamlessly design, simulate, analyze, implement, and test new process control algorithms in this multi-DSP environment. When successfully implemented, such tools would allow control system engineers to model the system in commercial off the shelf software (COTS), such as MatLab or LabView, and then download executable code to the target system for run-time test and analysis. This would open up the range of applications which would directly benefit from this research.

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